Technical Information Document

Sunny Central UP (-US)

Agenda

1. Efficiency

The conversion efficiency of the inverter is defined by the ratio of AC output power to DC input power. The main losses occur as waste heat due to switching and conducting losses inside the IGBT's of the inverter and due to the inductance of the sine filter choke. Depending on the methodology of measuring the efficiency, the self-consumption of the inverter can also be integrated into the efficiency calculation as it is done with the CEC efficiency rating.

The conversion efficiency strongly depends on the DC voltage with the highest efficiency being experienced at the lowest possible DC voltage for this type of inverter bridge topology.

a) Efficiency without auxiliary losses

Figure 1: Efficiency without aux. losses at 25°C measured according to IEC 61683

Figure 2: Efficiency without aux. losses at 25°C measured according to IEC 61683

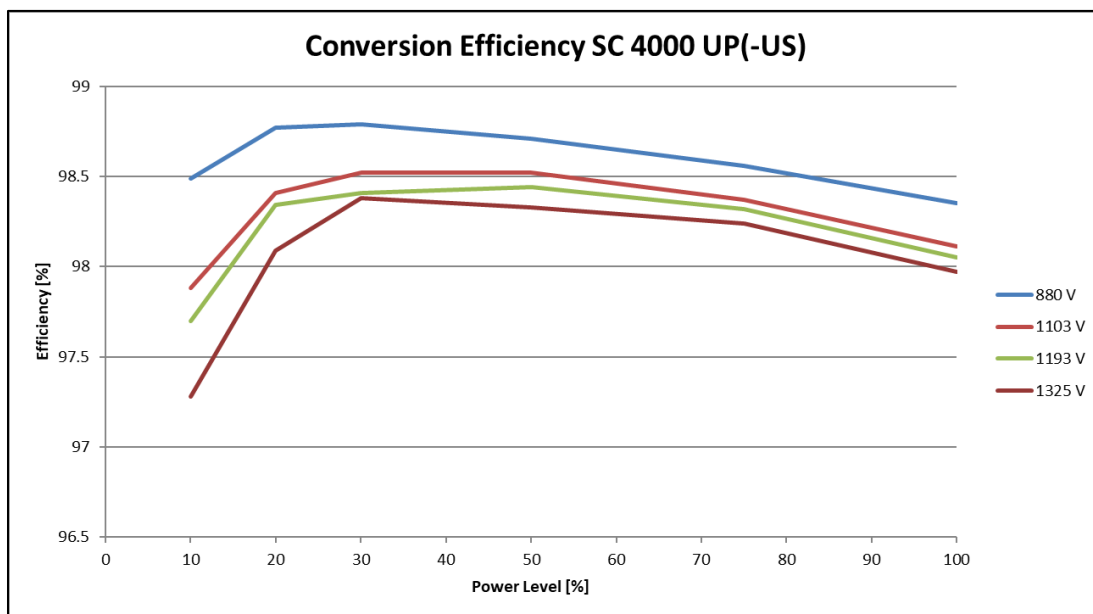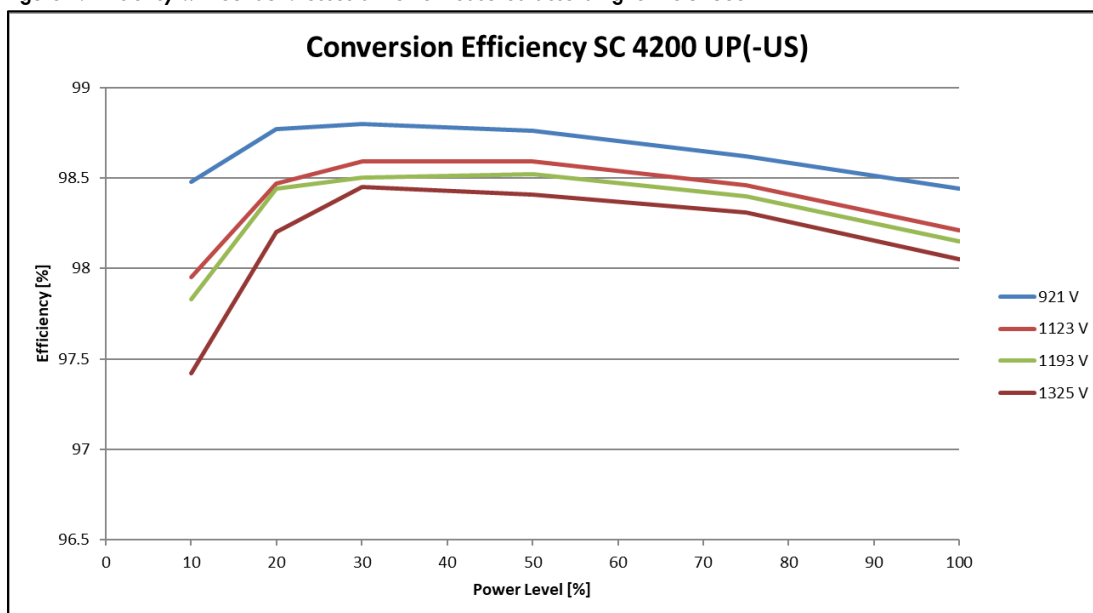Figure 3: Efficiency without aux. losses at 25°C measured according to IEC 61683

Figure 4: Efficiency without aux. losses at 25°C measured according to IEC 61683
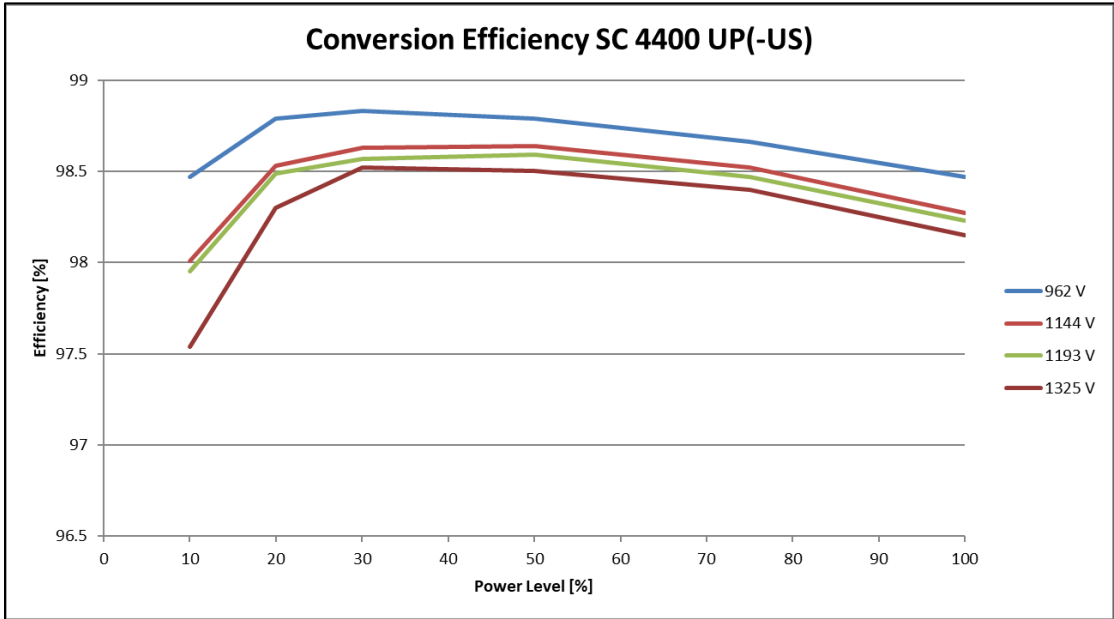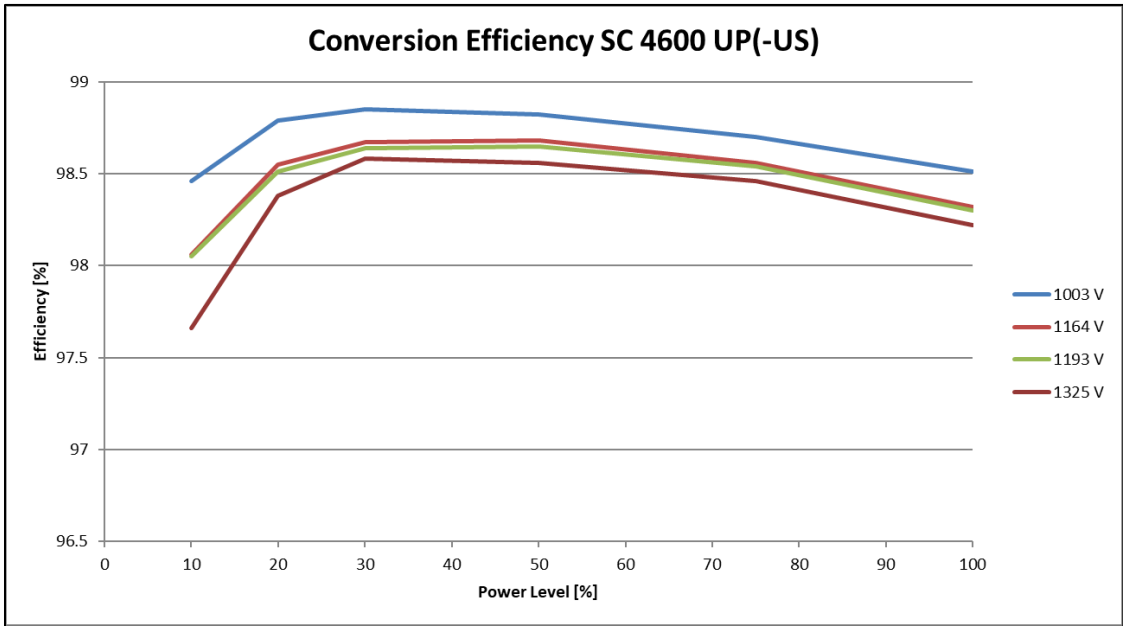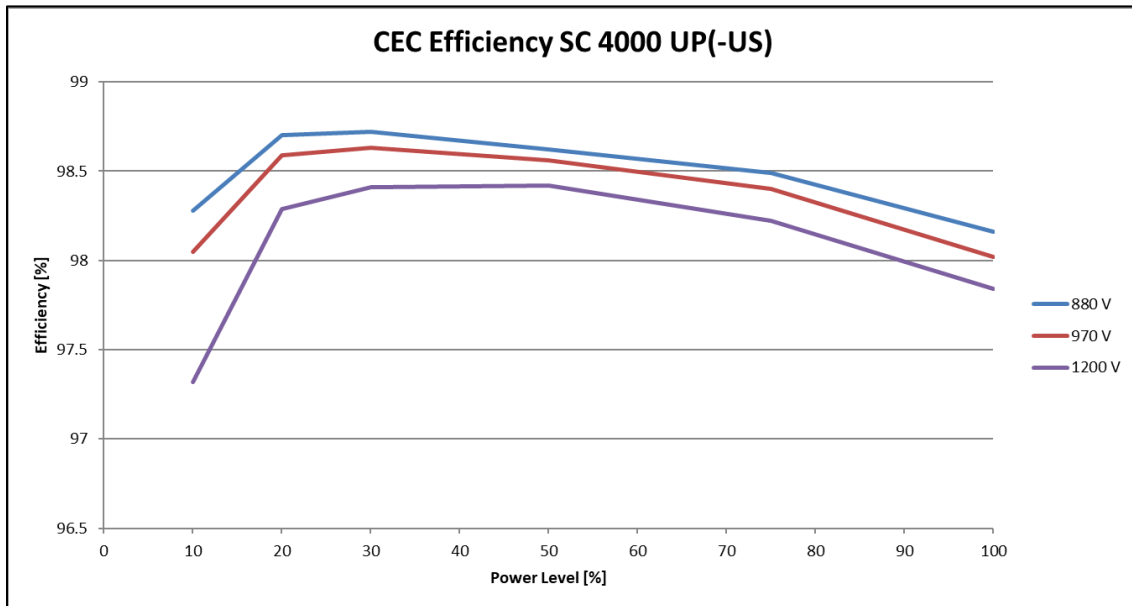
b) Efficiency with auxiliary losses

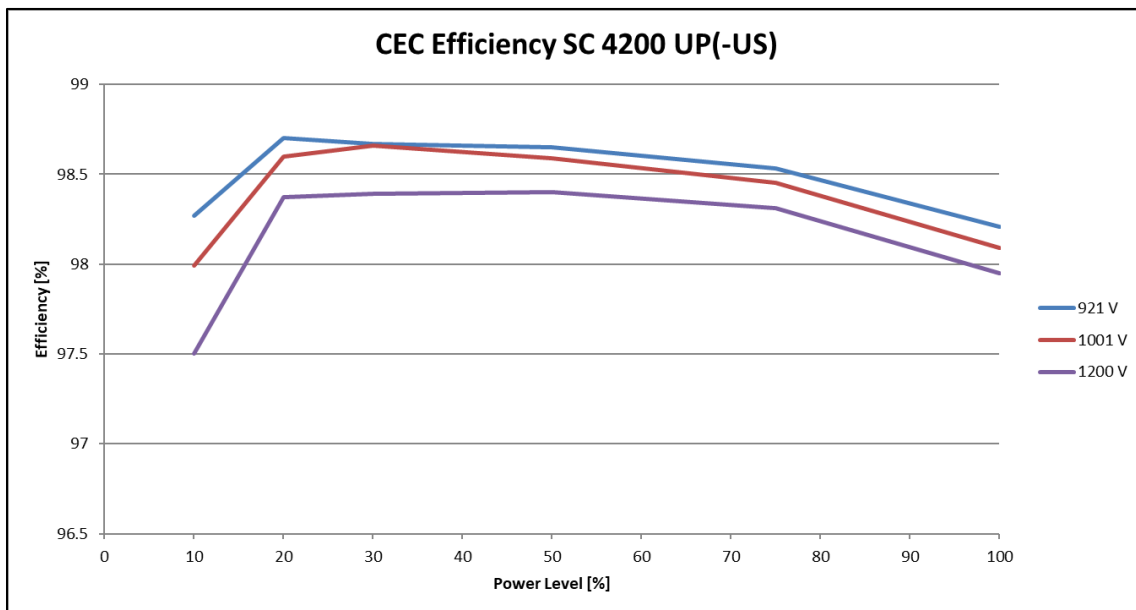Figure 5: Efficiency with aux. losses at 25°C
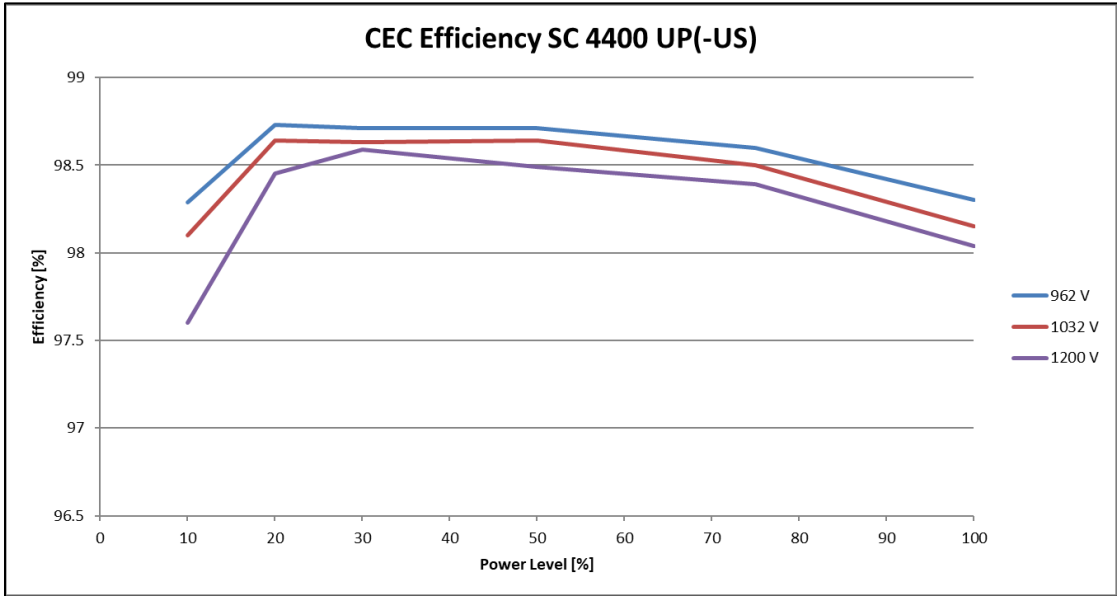

Figure 6: Efficiency with aux. losses at 25°C
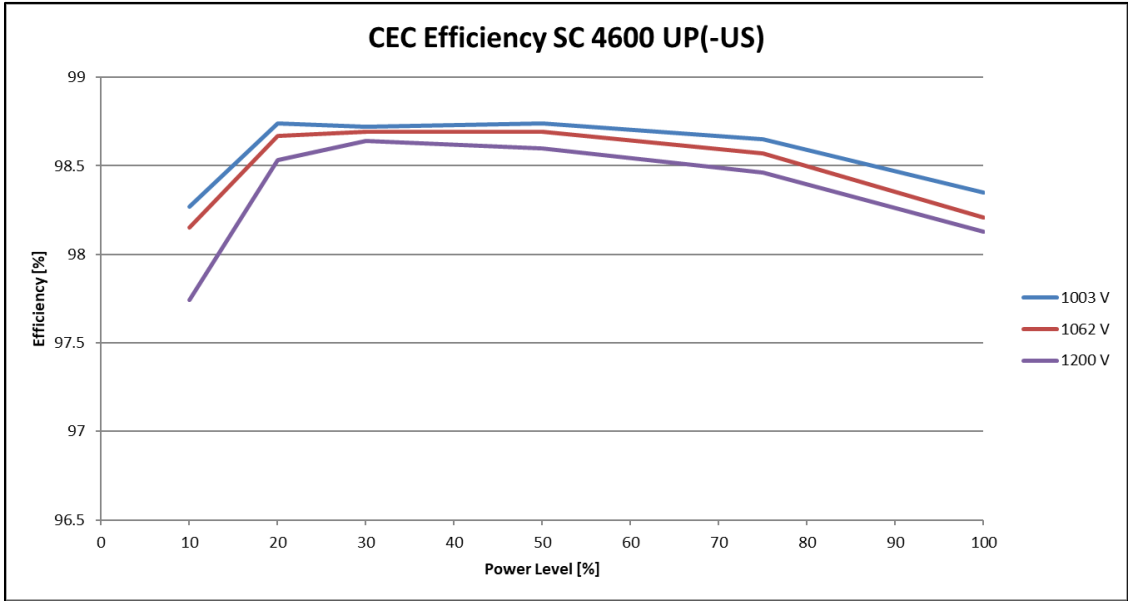
Figure 7: Efficiency with aux. losses at 25°C

Figure 8: Efficiency with aux. losses at 25°C

c) Calculated CEC & EuroETA efficiency

CEC Efficiency with Aux losses SC 4000 UP(-US)

VDC\PAC	10%	20%	30%	50%	75%	100%	CEC
880 V	98.28%	98.70%	98.72%	98.62%	98.49%	98.16%	98.53%
970 V	98.05%	98.59%	98.63%	98.56%	98.40%	98.02%	98.44%
1200 V	97.32%	98.29%	98.41%	98.42%	98.22%	97.84%	98.23%
							98.40%

CEC Efficiency with Aux losses SC 4200 UP(-US)

VDC\PAC	10%	20%	30%	50%	75%	100%	CEC
921 V	98.27%	98.70%	98.67%	98.65%	98.53%	98.21%	98.55%
1001 V	97.99%	98.60%	98.66%	98.59%	98.45%	98.09%	98.48%
1200 V	97.50%	98.37%	98.39%	98.40%	98.31%	97.95%	98.29%
							98.44%

CEC Efficiency with Aux losses SC 4400 UP(-US)

VDC\PAC	10%	20%	30%	50%	75%	100%	CEC
962 V	98.29%	98.73%	98.71%	98.71%	98.60%	98.30%	98.62%
1032 V	98.10%	98.64%	98.63%	98.64%	98.50%	98.15%	98.52%
1200 V	97.60%	98.45%	98.59%	98.49%	98.39%	98.04%	98.39%
							98.51%

CEC Efficiency with Aux losses SC 4600 UP(-US)

VDC\PAC	10%	20%	30%	50%	75%	100%	CEC
1003 V	98.27%	98.74%	98.72%	98.74%	98.65%	98.35%	98.65%
1062 V	98.15%	98.67%	98.69%	98.69%	98.57%	98.21%	98.58%
1200 V	97.74%	98.53%	98.64%	98.60%	98.46%	98.13%	98.47%
							98.57%

Table 1: Calculated CEC efficiency with Aux losses

Conversion Efficiency SC 4000 UP(-US) (IEC 61683)

VDC\PAC	5%	10%	20%	30%	50%	75%	100%	EuroETA
880 V	97.75%	98.49%	98.77%	98.79%	98.71%	98.56%	98.35%	98.61%
1103 V	96.54%	97.88%	98.41%	98.52%	98.52%	98.37%	98.11%	98.33%
1193 V	96.07%	97.70%	98.34%	98.41%	98.44%	98.32%	98.05%	98.23%
1325 V	95.18%	97.28%	98.09%	98.38%	98.33%	98.24%	97.97%	98.07%

Conversion Efficiency SC 4200 UP(-US) (IEC 61683)

VDC\PAC	5%	10%	20%	30%	50%	75%	100%	EuroETA
921 V	97.71%	98.48%	98.77%	98.80%	98.76%	98.62%	98.44%	98.65%
1123 V	96.66%	97.95%	98.47%	98.59%	98.59%	98.46%	98.21%	98.40%
1193 V	96.32%	97.83%	98.44%	98.50%	98.52%	98.40%	98.15%	98.33%
1325 V	95.44%	97.42%	98.20%	98.45%	98.41%	98.31%	98.05%	98.17%

Conversion Efficiency SC 4400 UP(-US) (IEC 61683)

VDC\PAC	5%	10%	20%	30%	50%	75%	100%	EuroETA
962 V	97.68%	98.47%	98.79%	98.83%	98.79%	98.66%	98.47%	98.68%
1144 V	96.77%	98.01%	98.53%	98.63%	98.64%	98.52%	98.27%	98.46%
1193 V	96.55%	97.95%	98.49%	98.57%	98.59%	98.47%	98.23%	98.40%
1325 V	95.70%	97.54%	98.30%	98.52%	98.50%	98.40%	98.15%	98.26%

Conversion Efficiency SC 4600 UP(-US) (IEC 61683)

VDC\PAC	5%	10%	20%	30%	50%	75%	100%	EuroETA
1003 V	97.66%	98.46%	98.79%	98.85%	98.82%	98.70%	98.51%	98.70%
1164 V	96.86%	98.06%	98.55%	98.67%	98.68%	98.56%	98.32%	98.50%
1193 V	96.77%	98.05%	98.51%	98.64%	98.65%	98.54%	98.30%	98.47%
1325 V	95.94%	97.66%	98.38%	98.58%	98.56%	98.46%	98.22%	98.34%

Table 2: Calculated EutoETA efficiency without Aux losses

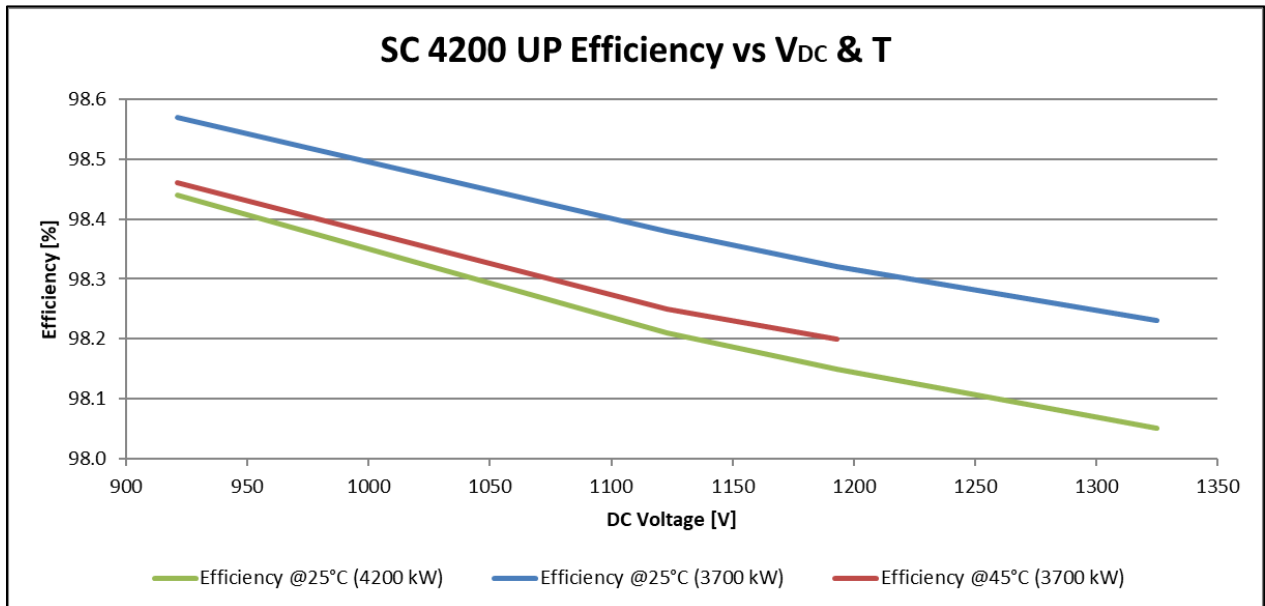## d) Efficiency at higher ambient temperature

Figure 9: Conversion efficiency at different temperature and DC voltage

e) Efficiency in dependence of Power Factor

Available in January 2020

Figure 10: Efficiency in dependence of Power Factor

2. Auxiliary Consumption

The inverter converts DC to AC power which requires some auxiliary power for the control, communication and cooling system. The amount of auxiliary power depends on the ambient temperature and on the produced output power. The auxiliary power is drawn from the AC side at the inverter terminals.

If the available PV power exceeds 100% of the DC power which can be converted by the inverter per nameplate rating, the inverter produces some more AC power in order to compensate for its internal losses. That way the effective auxiliary consumption of the inverter is 0 kVA as soon as the DC power exceeds 100%.

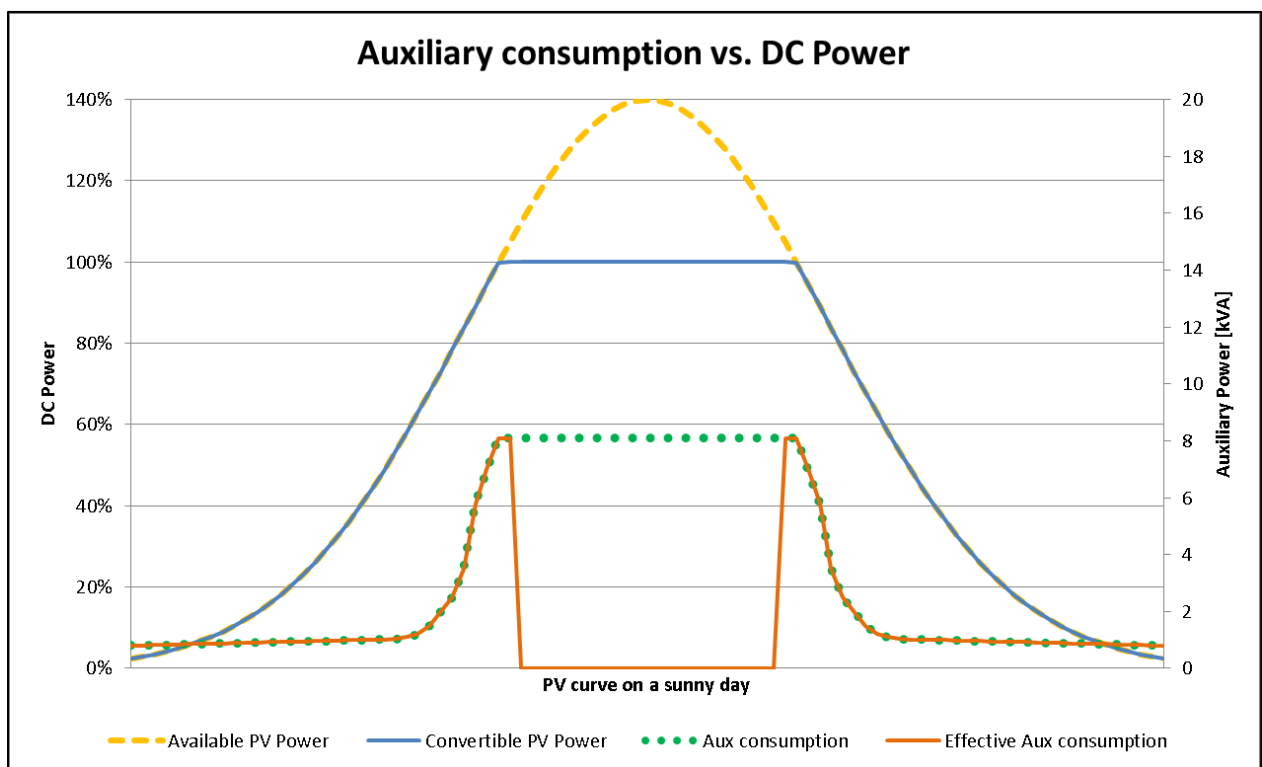## a) Auxiliary consumption on a sunny day

Figure 11: Auxiliary power consumption on a sunny day at 25°C

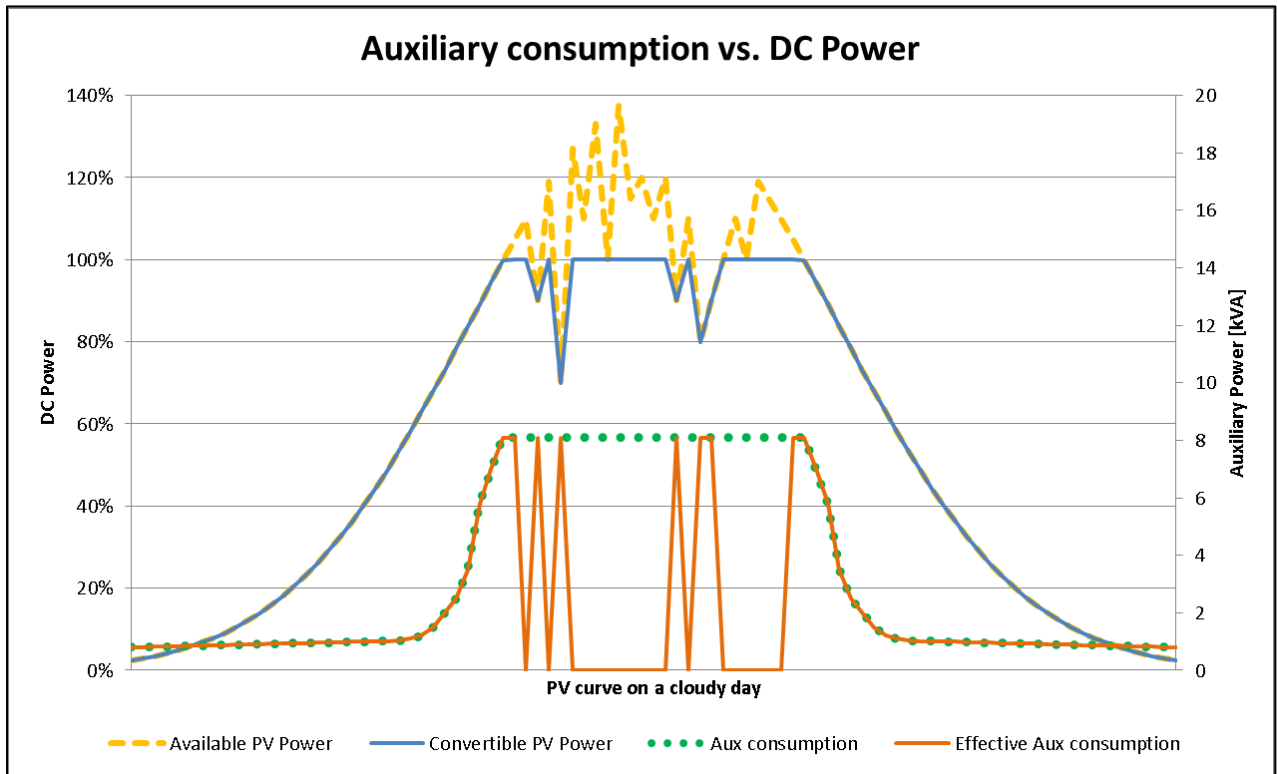## b) Auxiliary consumption on a cloudy day

Figure 12: Auxiliary power consumption on a cloudy day at 25°C

3. Harmonics

Harmonics occur as integer multiples of the fundamental frequency which is typically 50 Hz or 60 Hz in electronic power grids. Harmonic currents cause voltage drops which superimpose the nominal grid voltage resulting in distortion of the sine wave of the grid voltage. Harmonics can be generated by non-linear loads or from power electronic means with high frequent switching transistors (for example by an inverter).

The inverter control and the filter design have a big impact on the harmonics generated by the inverter. The measured harmonics will also vary with the grid frequency, the grid impedance and the initial level of harmonic stress in the grid.

The system solution which uses a Dy transformer for the connection to the MV grid has a different harmonic spectrum as the Delta winding of the transformer does not allow a zero sequence system to develop. Thus the corresponding harmonics (all multiples of the 3rd order) equal zero on the MV side. This effect is shown in Figure 9. Additionally the Sunny Central UP(-US) actively compensates harmonics up to the 7th order by its internal control, thus producing a total harmonic current (THC) of less than 1%.
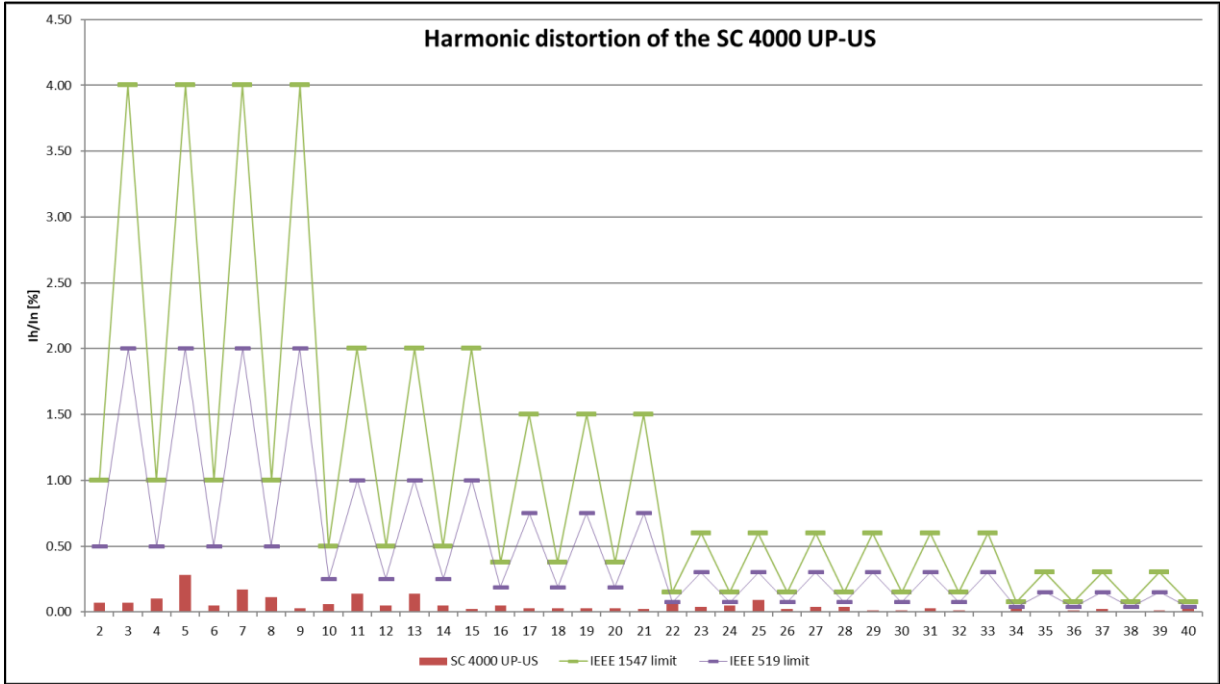
a) Measurements according to IEEE 1547 (60Hz)

Figure 13: Harmonic distortion compared to the limits defined by IEEE 1547 and IEEE 519

Order	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
L1 [%]	0.07	0.07	0.10	0.25	0.04	0.16	0.10	0.02	0.03	0.14	0.01	0.11	0.05	0.02	0.02	0.03	0.01	0.03	0.03	0.01
L2 [%]	0.07	0.04	0.09	0.28	0.05	0.13	0.10	0.03	0.04	0.12	0.05	0.10	0.03	0.02	0.03	0.01	0.03	0.01	0.01	0.02
L3 [%]	0.04	0.04	0.09	0.26	0.02	0.17	0.11	0.03	0.06	0.12	0.04	0.14	0.03	0.01	0.05	0.02	0.02	0.03	0.03	0.02
Order	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	TDD
L1 [%]	0.06	0.04	0.04	0.09	0.02	0.02	0.02	0.01	0.00	0.02	0.01	0.00	0.03	0.00	0.01	0.02	0.00	0.01	0.02	**0.42**
L2 [%]	0.03	0.03	0.05	0.05	0.02	0.04	0.03	0.01	0.01	0.03	0.01	0.00	0.03	0.00	0.01	0.02	0.00	0.00	0.03	**0.41**
L3 [%]	0.06	0.04	0.02	0.06	0.01	0.02	0.04	0.01	0.01	0.03	0.00	0.00	0.03	0.00	0.01	0.02	0.00	0.01	0.03	**0.43**

Table 3: Harmonic distortion of the SC 4000 UP(-US) per phase at 1325 V_{DC} and 100% P_{AC} (60 Hz)
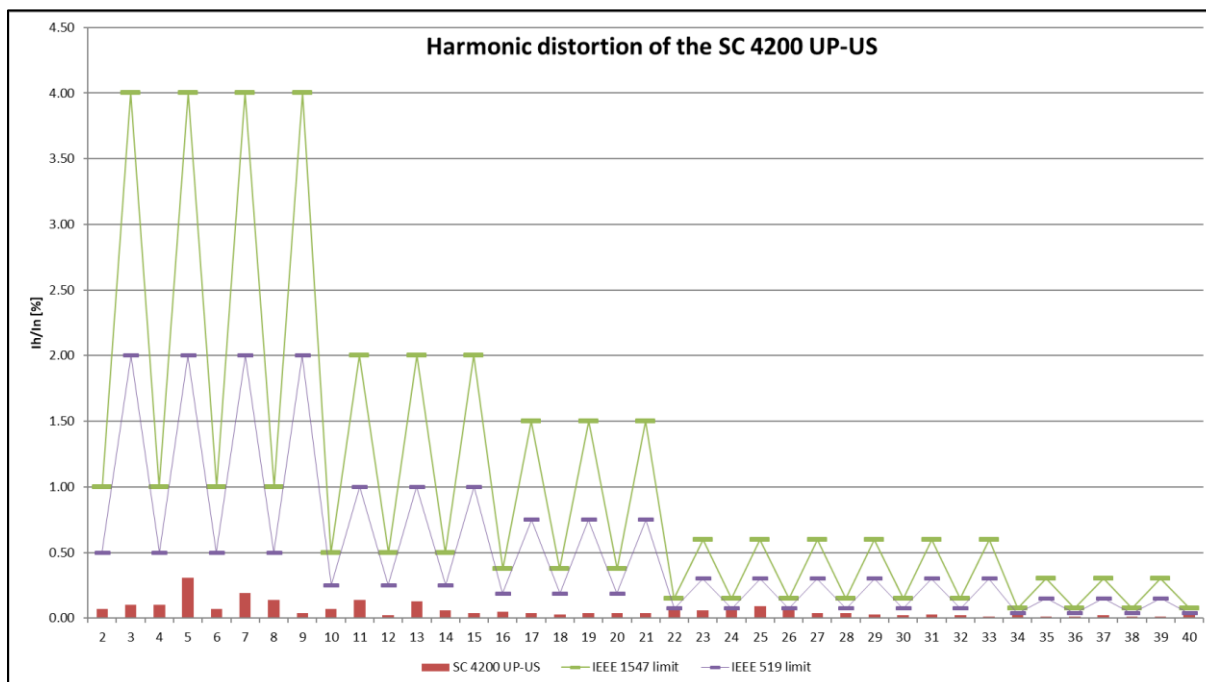
Figure 14: Harmonic distortion compared to the limits defined by IEEE 1547 and IEEE 519

Order	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
L1 [%]	0.07	0.06	0.10	0.26	0.02	0.19	0.10	0.01	0.07	0.13	0.02	0.12	0.04	0.01	0.04	0.02	0.01	0.04	0.03	0.01
L2 [%]	0.07	0.10	0.09	0.31	0.07	0.14	0.14	0.04	0.05	0.14	0.02	0.08	0.06	0.04	0.01	0.04	0.03	0.01	0.04	0.03
L3 [%]	0.02	0.05	0.09	0.28	0.05	0.18	0.12	0.04	0.07	0.14	0.01	0.13	0.04	0.03	0.05	0.03	0.03	0.02	0.04	0.04

Order	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	TDD
L1 [%]	0.06	0.03	0.04	0.09	0.04	0.00	0.04	0.01	0.02	0.03	0.01	0.00	0.02	0.01	0.01	0.02	0.00	0.01	0.02	**0.44**
L2 [%]	0.04	0.06	0.07	0.04	0.08	0.04	0.03	0.03	0.02	0.02	0.02	0.00	0.03	0.01	0.01	0.02	0.01	0.01	0.03	**0.48**
L3 [%]	0.03	0.04	0.03	0.05	0.05	0.04	0.01	0.02	0.01	0.02	0.01	0.01	0.03	0.01	0.01	0.02	0.01	0.01	0.03	**0.45**

Table 4: Harmonic distortion of the SC 4200 UP(-US) per phase at 1325 V$_{DC}$ and 100% P$_{AC}$ (60 Hz)
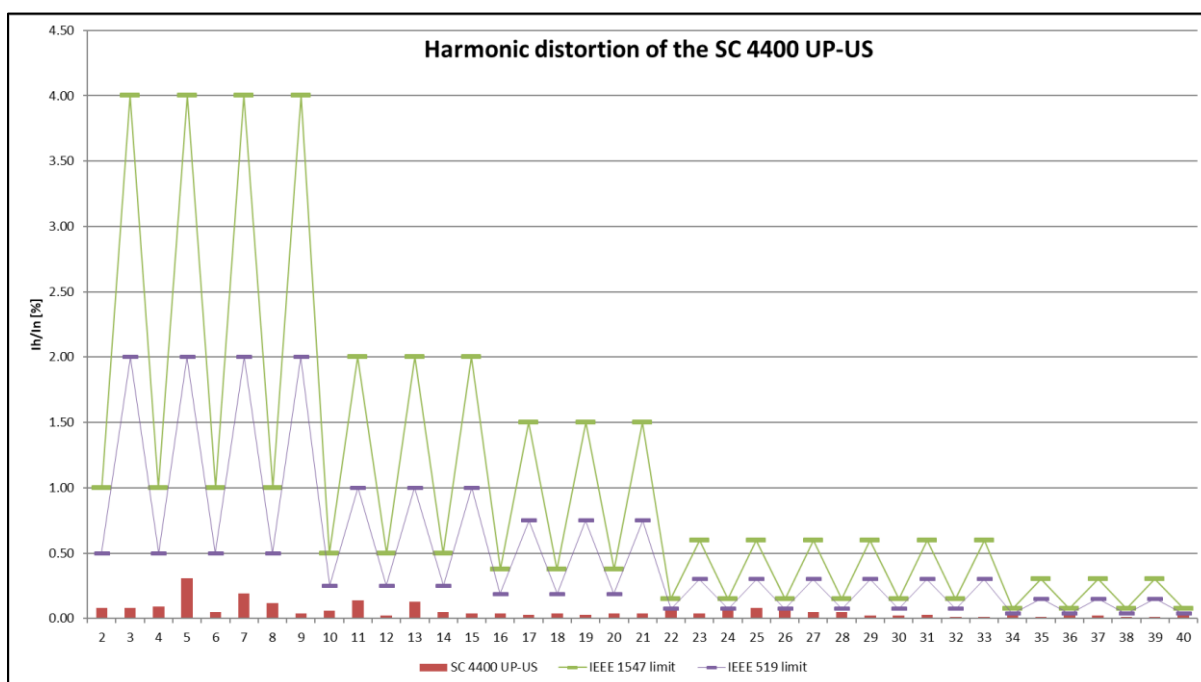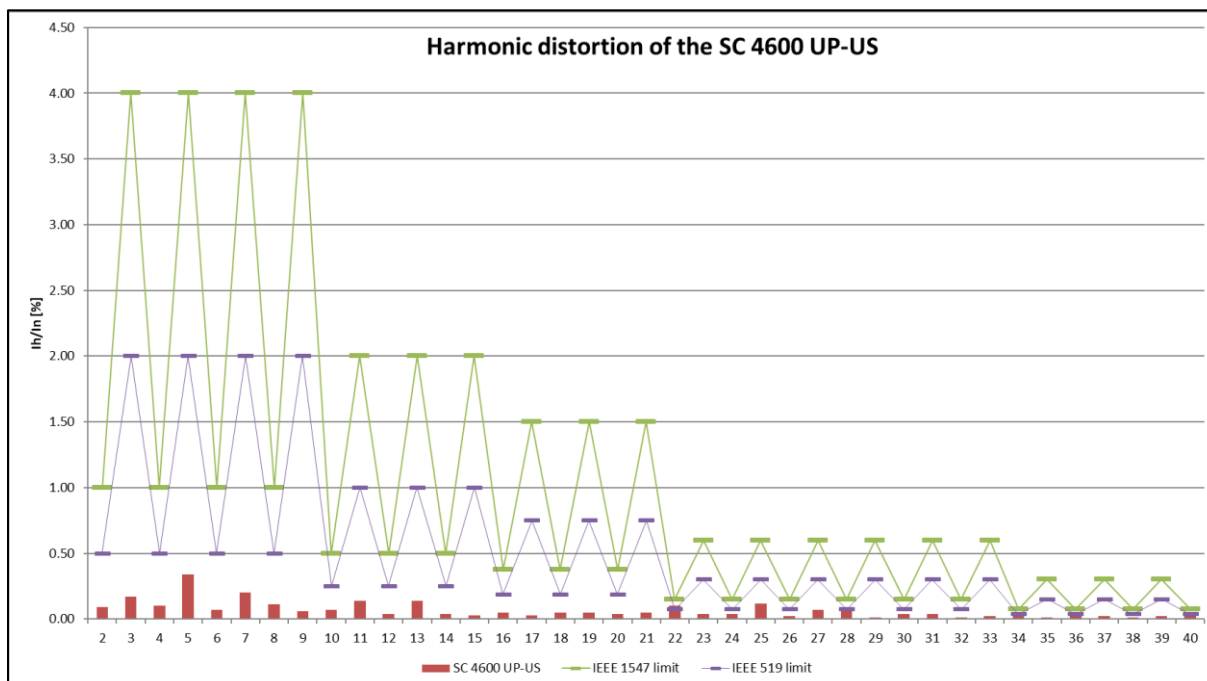
Figure 15: Harmonic distortion compared to the limits defined by IEEE 1547 and IEEE 519

Order	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
L1 [%]	0.08	0.08	0.09	0.26	0.01	0.19	0.10	0.02	0.06	0.13	0.02	0.12	0.04	0.01	0.04	0.02	0.02	0.03	0.03	0.02
L2 [%]	0.07	0.06	0.09	0.31	0.03	0.15	0.12	0.02	0.05	0.14	0.02	0.07	0.05	0.04	0.01	0.03	0.02	0.01	0.03	0.02
L3 [%]	0.06	0.03	0.09	0.27	0.05	0.18	0.11	0.04	0.06	0.13	0.02	0.13	0.04	0.03	0.04	0.02	0.04	0.02	0.04	0.04
Order	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	TDD
L1 [%]	0.07	0.03	0.01	0.08	0.03	0.02	0.05	0.01	0.02	0.03	0.01	0.01	0.02	0.01	0.02	0.02	0.00	0.01	0.02	**0.45**
L2 [%]	0.03	0.04	0.06	0.03	0.06	0.04	0.03	0.02	0.01	0.02	0.01	0.00	0.02	0.01	0.01	0.02	0.00	0.01	0.02	**0.46**
L3 [%]	0.06	0.04	0.05	0.06	0.04	0.05	0.03	0.02	0.01	0.02	0.01	0.01	0.02	0.01	0.02	0.02	0.01	0.01	0.03	**0.45**

Table 5: Harmonic distortion of the SC 4400 UP(-US) per phase at 1325 V_{DC} and 100% P_{AC} (60 Hz)

Figure 16: Harmonic distortion compared to the limits defined by IEEE 1547 and IEEE 519

Order	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
L1 [%]	0.08	0.17	0.09	0.26	0.07	0.20	0.10	0.06	0.07	0.12	0.03	0.14	0.03	0.03	0.05	0.01	0.05	0.05	0.03	0.05
L2 [%]	0.09	0.16	0.09	0.34	0.05	0.17	0.11	0.04	0.07	0.14	0.04	0.07	0.03	0.02	0.03	0.02	0.04	0.04	0.01	0.04
L3 [%]	0.08	0.04	0.10	0.27	0.02	0.18	0.10	0.02	0.06	0.13	0.01	0.12	0.04	0.01	0.03	0.03	0.03	0.01	0.04	0.03

Order	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	TDD
L1 [%]	0.10	0.02	0.04	0.12	0.02	0.07	0.09	0.01	0.04	0.04	0.01	0.02	0.03	0.00	0.02	0.02	0.01	0.02	0.02	**0.52**
L2 [%]	0.06	0.02	0.01	0.08	0.01	0.06	0.08	0.01	0.03	0.04	0.00	0.01	0.02	0.00	0.02	0.01	0.00	0.01	0.02	**0.51**
L3 [%]	0.05	0.04	0.03	0.05	0.02	0.04	0.03	0.01	0.01	0.02	0.01	0.01	0.02	0.01	0.02	0.02	0.00	0.02	0.02	**0.44**

Table 6: Harmonic distortion of the SC 4600 UP(-US) per phase at 1325 V_{DC} and 100% P_{AC} (60 Hz)

b) Measurements according to VDE AR-N 4110 (50Hz)
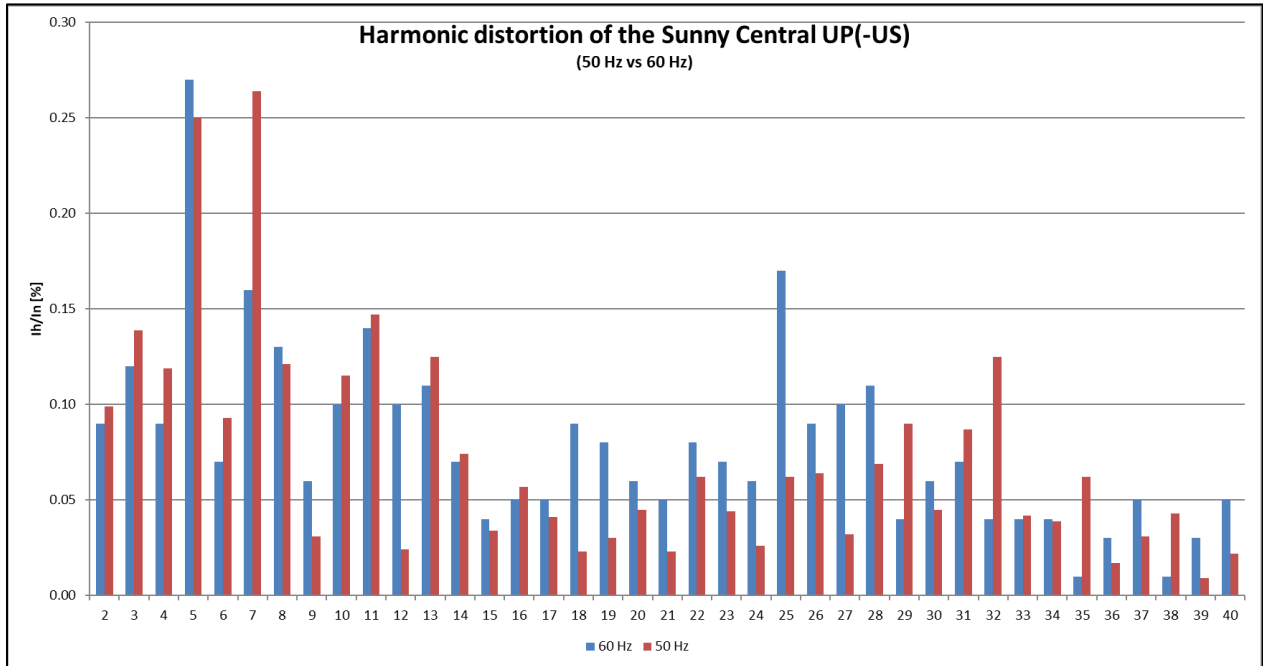
Figure 17: Harmonic distortion comparison at 50Hz and 60Hz grid frequency (measured at a SC 4400 UP)

Data of other power classes available in April 2020

Order	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Iv/In [%]	0.10	0.14	0.12	0.25	0.09	0.26	0.12	0.03	0.12	0.15	0.02	0.13	0.07	0.03	0.06	0.04	0.02
Order	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
Iv/In [%]	0.03	0.05	0.02	0.06	0.04	0.03	0.06	0.06	0.03	0.07	0.09	0.05	0.09	0.13	0.04	0.04	0.06
Order	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	THC	
Iv/In [%]	0.02	0.03	0.04	0.01	0.02	0.03	0.01	0.02	0.02	0.01	0.03	0.03	0.00	0.03	0.04	**0.58**	

Table 7: Total Harmonic distortion at 100% P$_{AC}$ (50 Hz)

4. Reactive Power

The inverter can provide reactive power in addition to the active power which is produced by conversion of incoming DC power. The resulting apparent power which is defined by the inverter's nameplate rating is calculated by geometric addition of reactive and active power.

The reactive power provision can be defined either via Power Factor (max. cosφ=0.8) or as a fix Q value. Since the reactive power is independent of the active power provision of the inverter, it is possible to provide the max. reactive power at any time respecting the limits defined by the apparent power value of the inverter at different ambient temperatures. The inverter can provide up to 60% of its nameplate rating as reactive power disconnecting only when the active power drops below 2 kW.

Reactive power has an impact on the frequency-dependent voltage drop at the sinus filter choke so that the minimum MPP voltage depends on the applied power factor. This effect is illustrated in the below pictures.

a) P/Q diagram Sunny Central UP @25°C
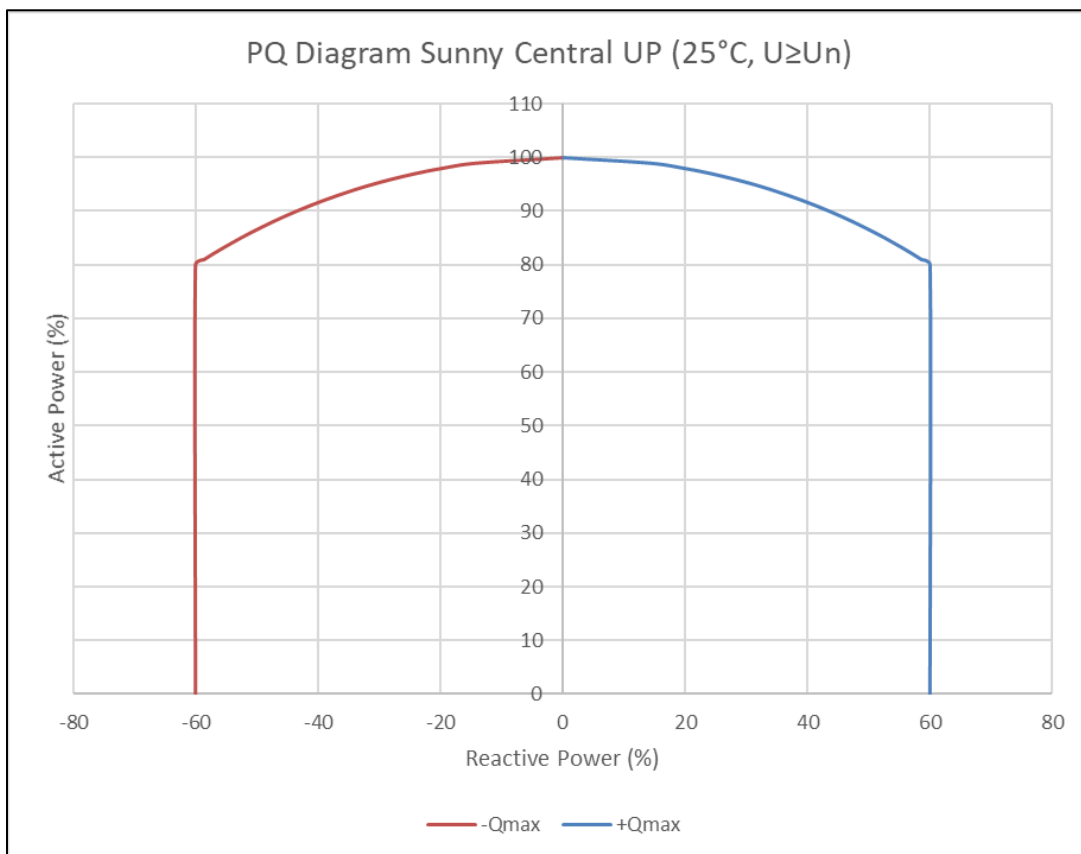
Figure 18: P/Q diagram at 25°C and grid voltage U ≥Un
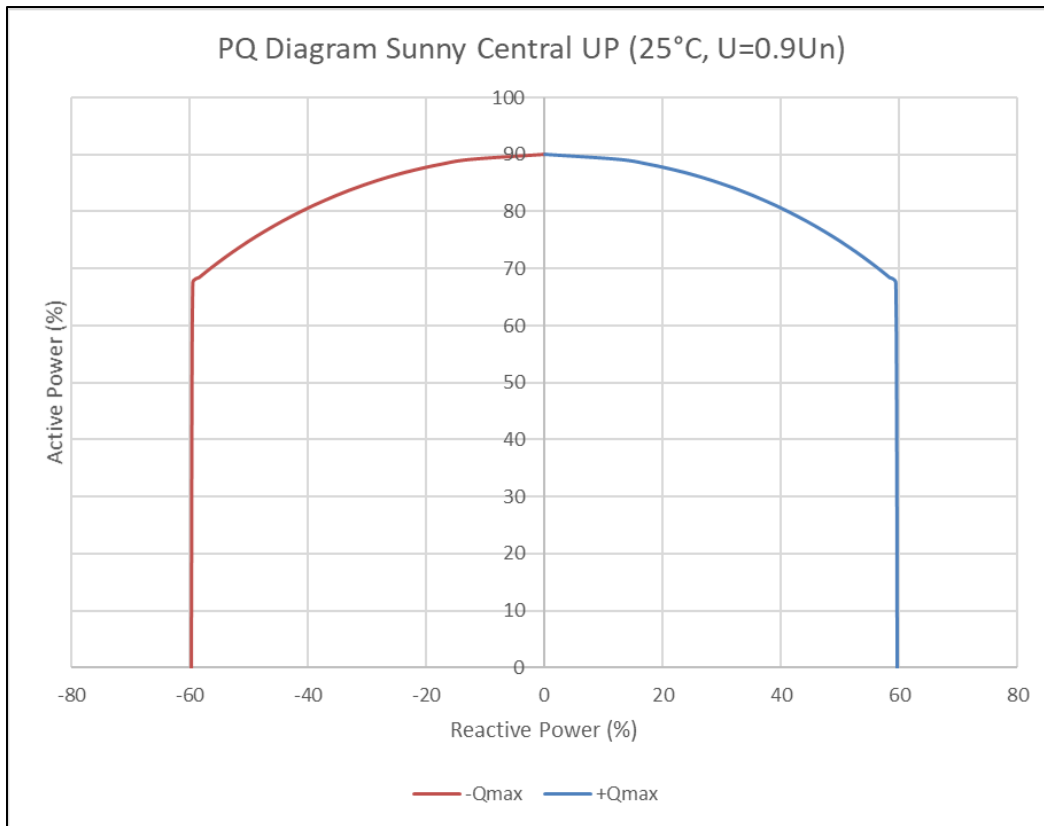
Figure 19: P/Q diagram at 25°C and grid voltage U = 0.9Un

b) P/Q diagram Sunny Central UP @40°C

PQ Diagram Sunny Central UP (40°C, U≥Un)

Active Power (%) vs Reactive Power (%)
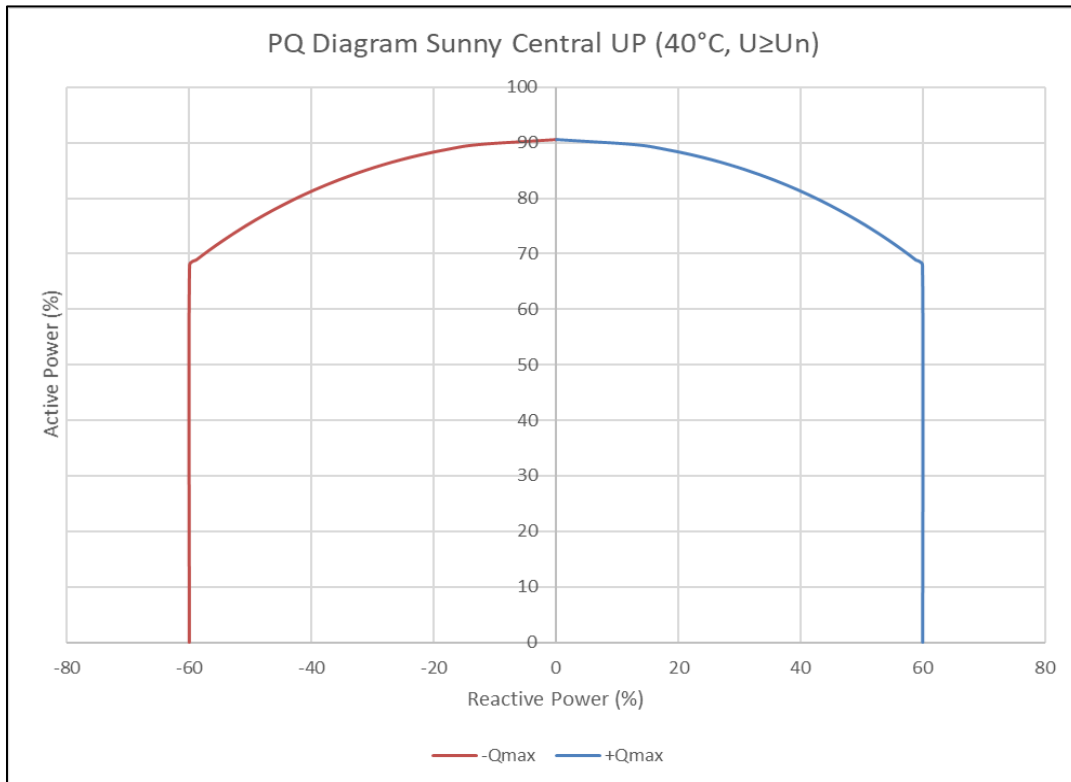
Figure 20: P/Q diagram at 40°C and grid voltage U ≥Un

PQ Diagram Sunny Central UP (40°C, U=0.9Un)

Active Power (%) vs Reactive Power (%)
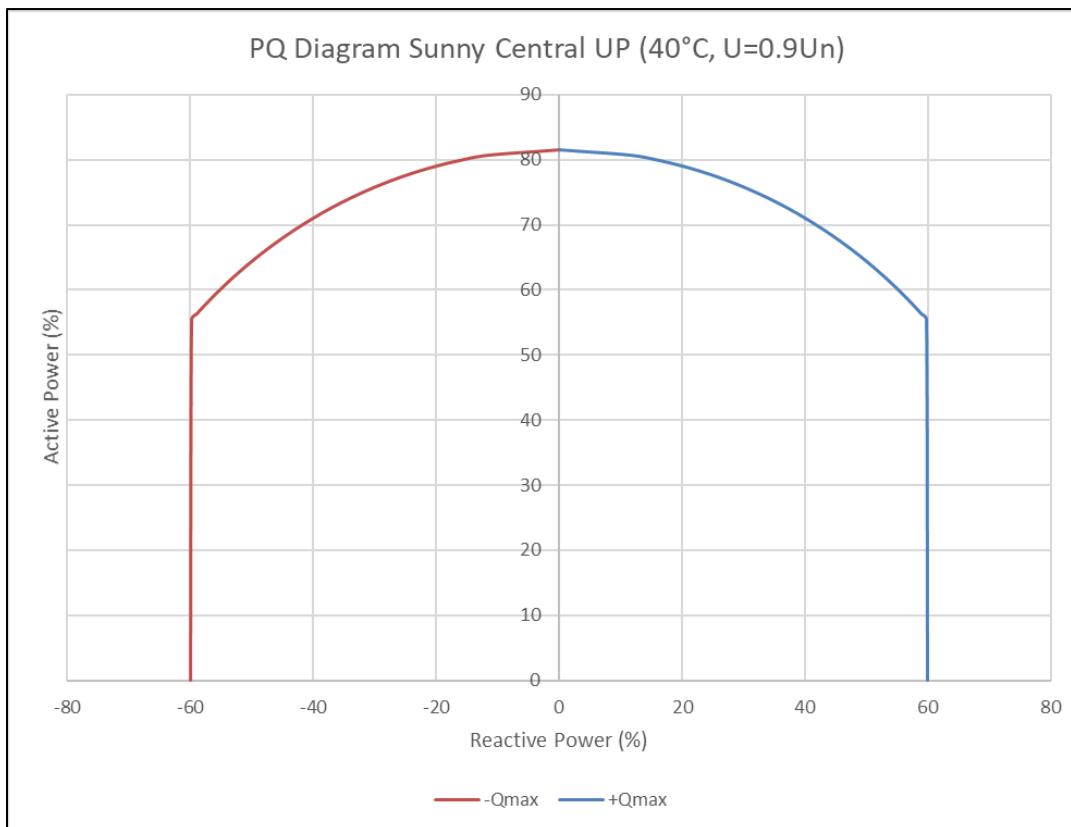
Figure 21: P/Q diagram at 40°C and grid voltage U =0.9Un

c) P/Q diagram Sunny Central UP @50°C
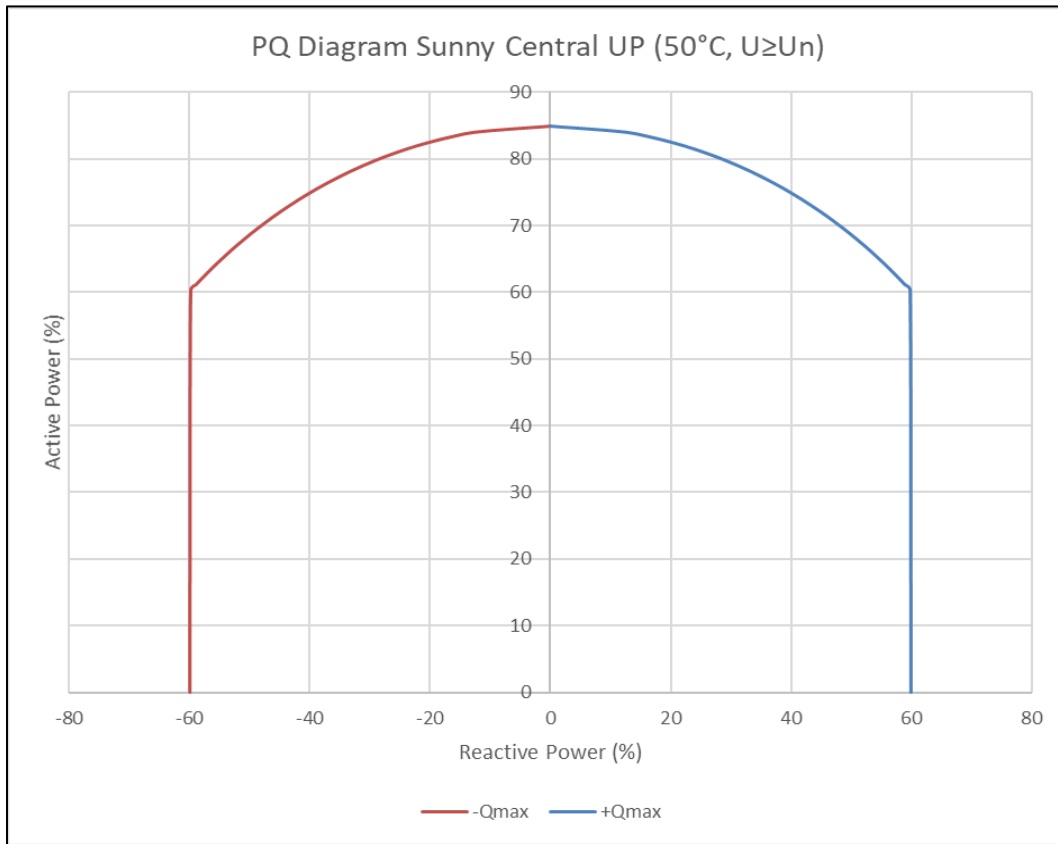
Figure 22: P/Q diagram at 50°C and grid voltage U ≥Un
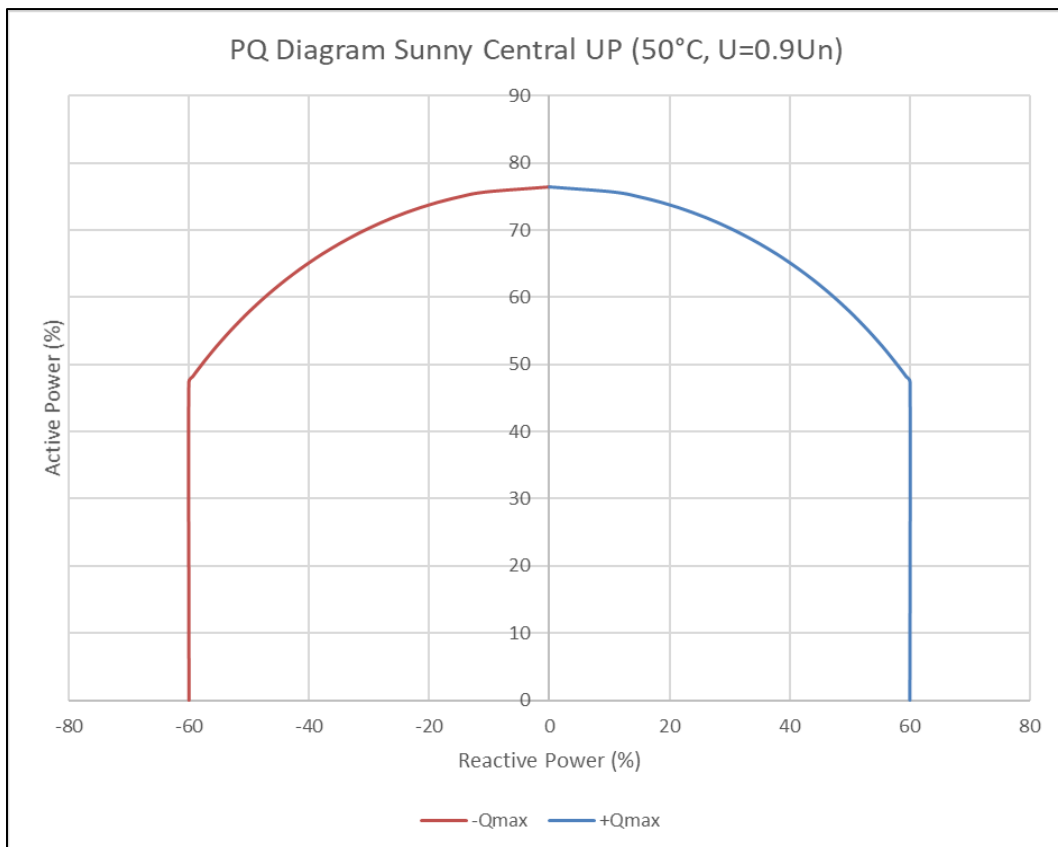
Figure 23: P/Q diagram at 50°C and grid voltage U =0.9Un

d) Minimum MPP Voltage with reactive power @60 Hz
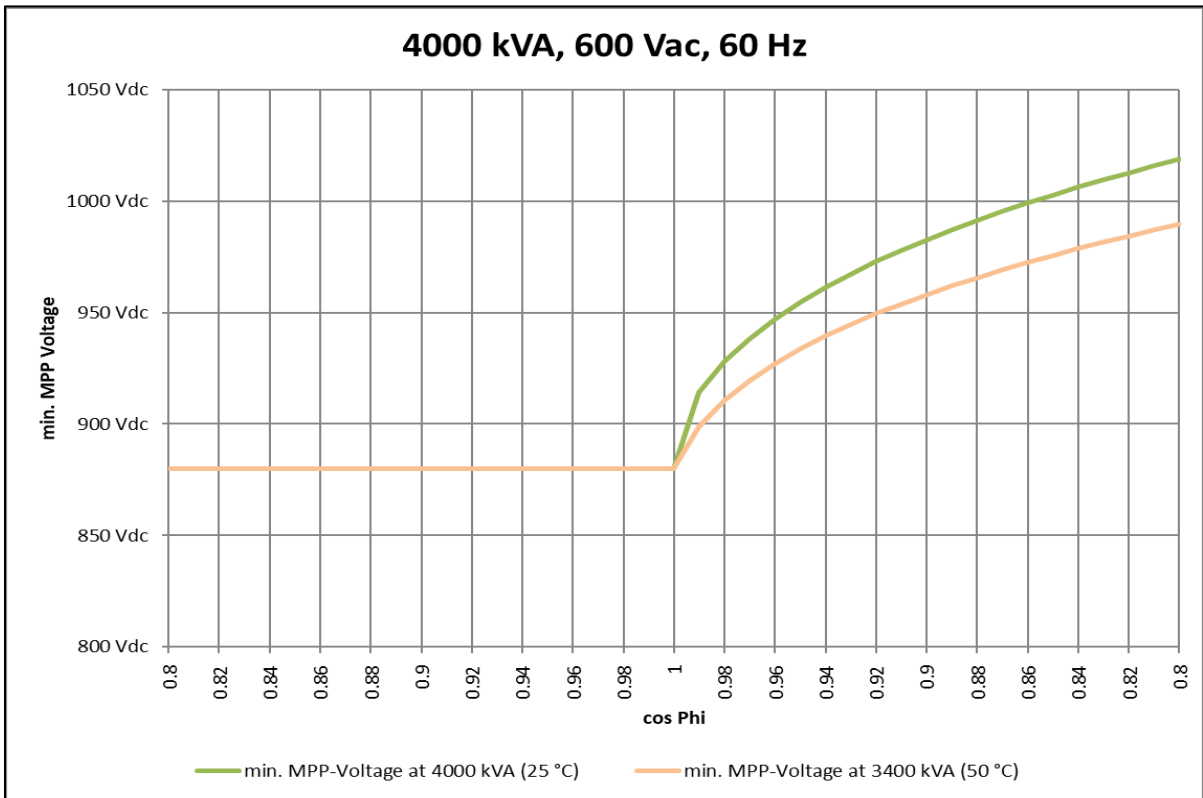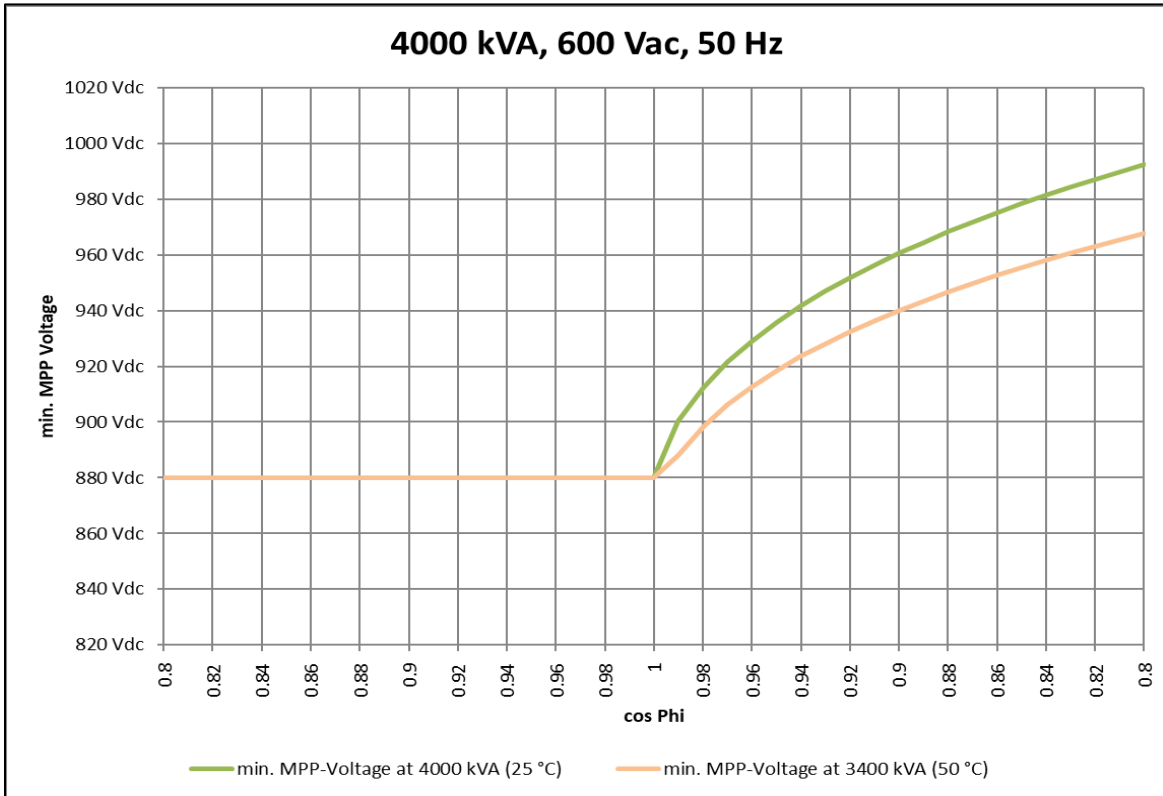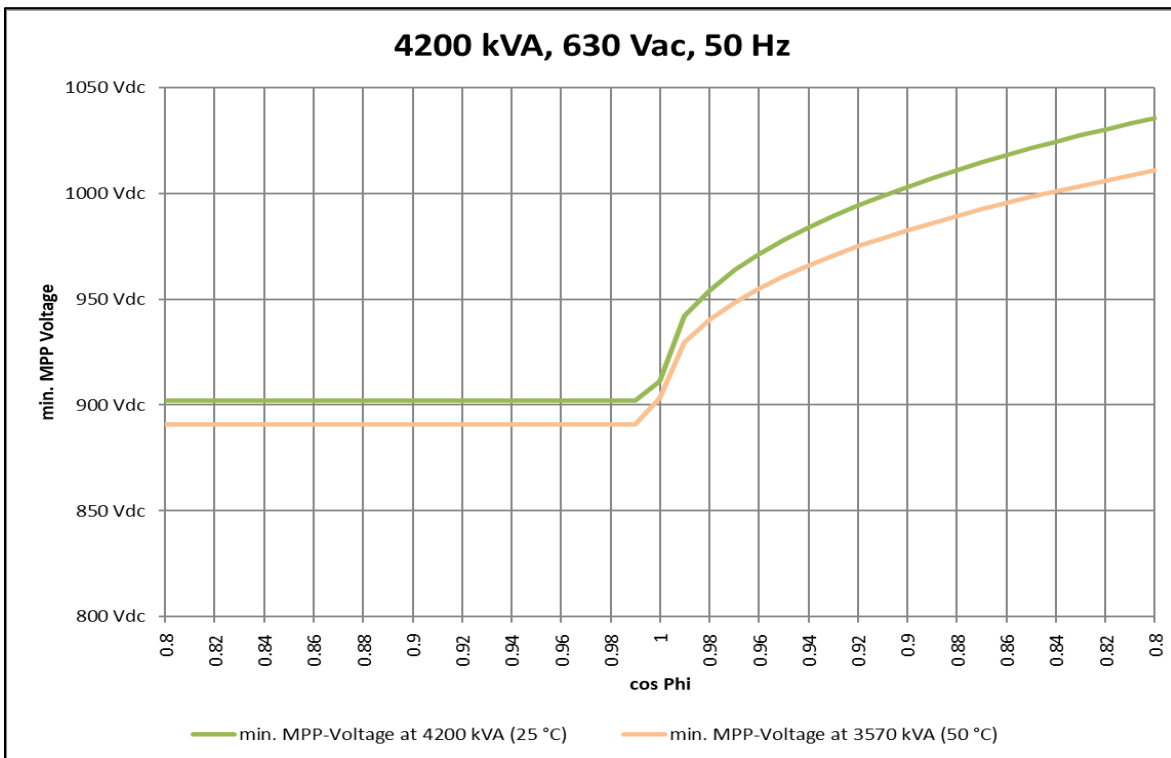

Figure 24: Minimum MPP Voltage of SC 4000 UP(-US) at 60 Hz
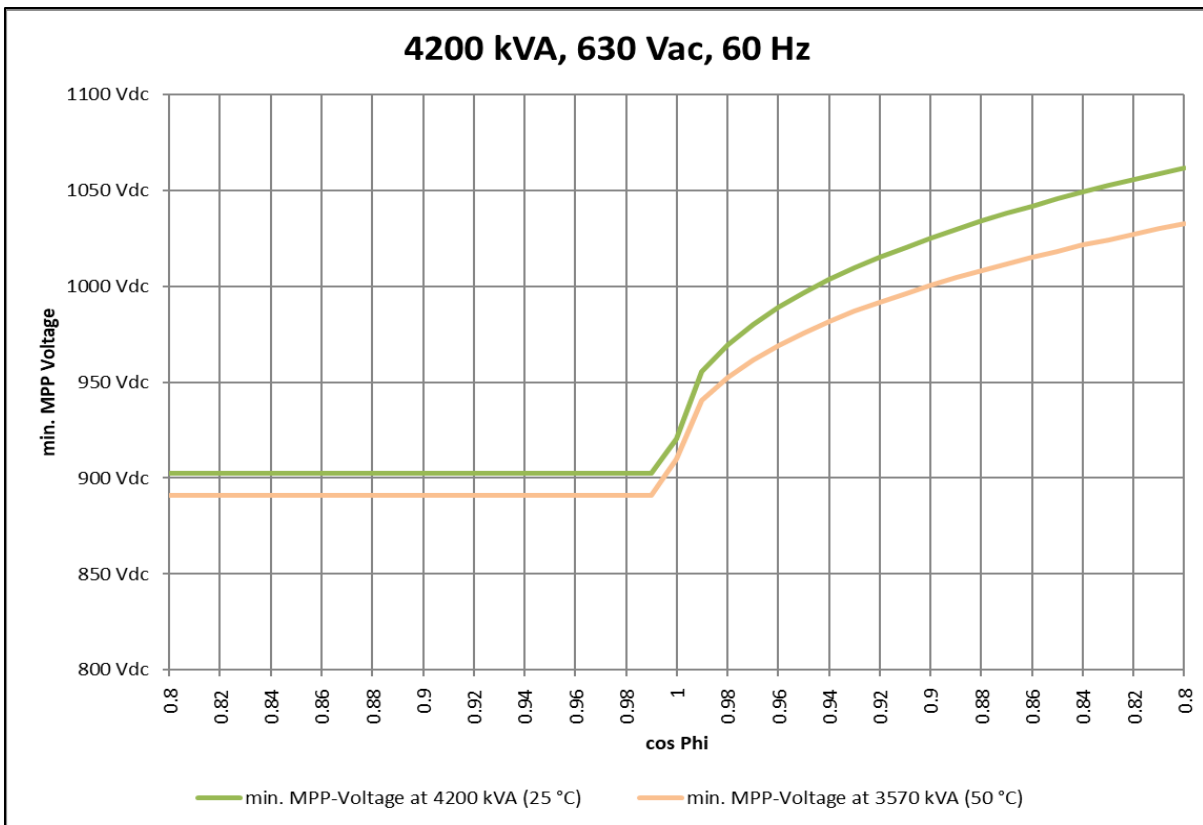
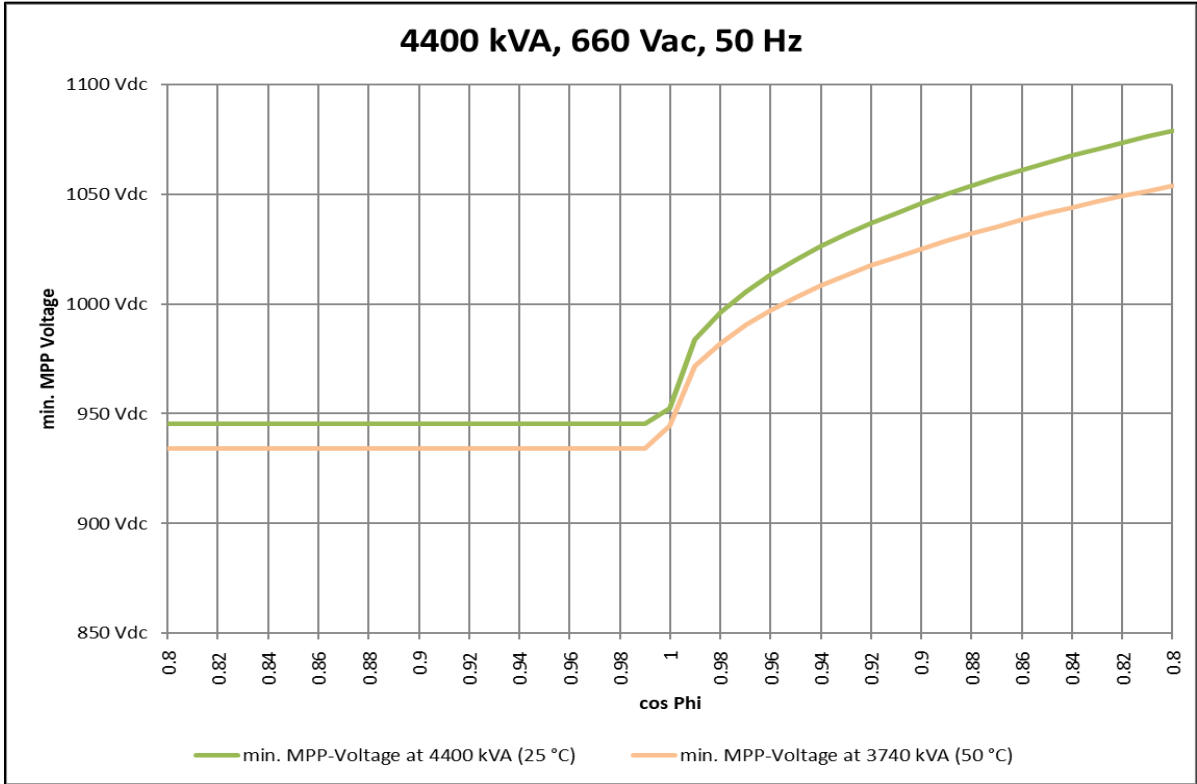Figure 25: Minimum MPP Voltage of SC 4200 UP(-US) at 60 Hz
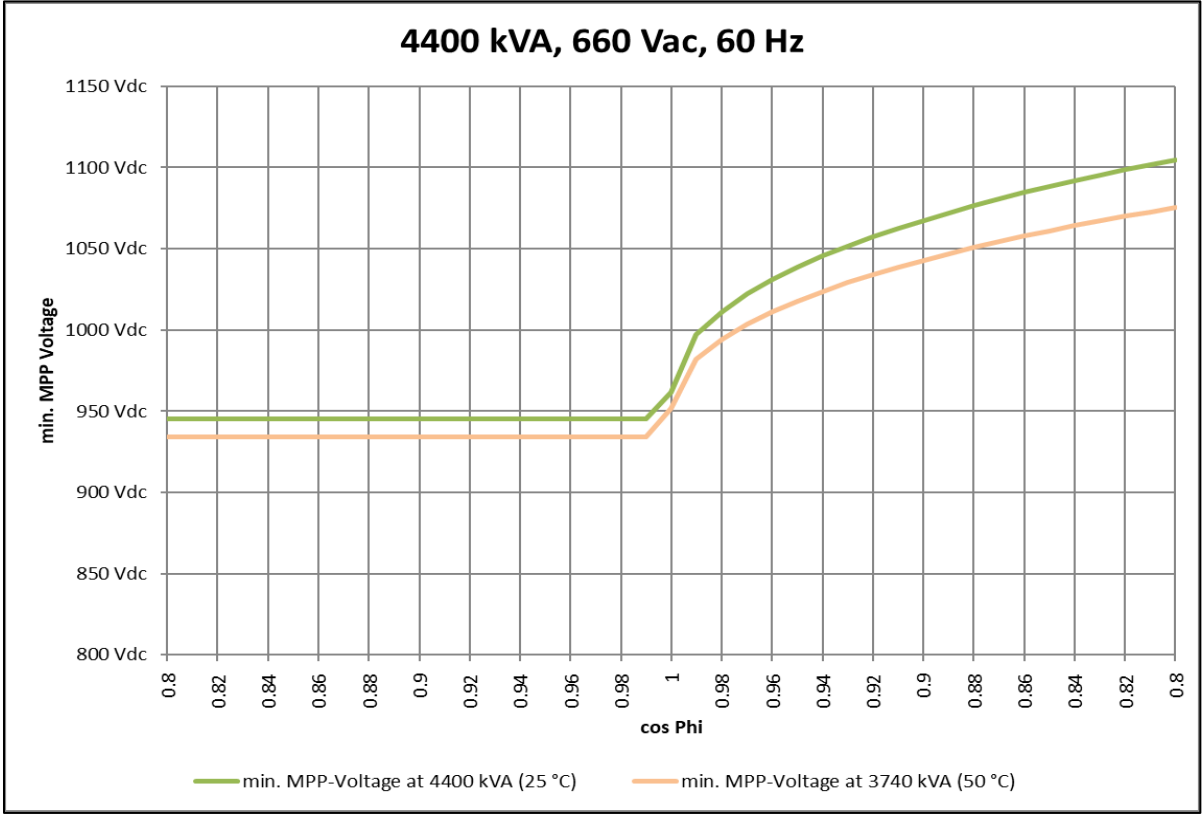
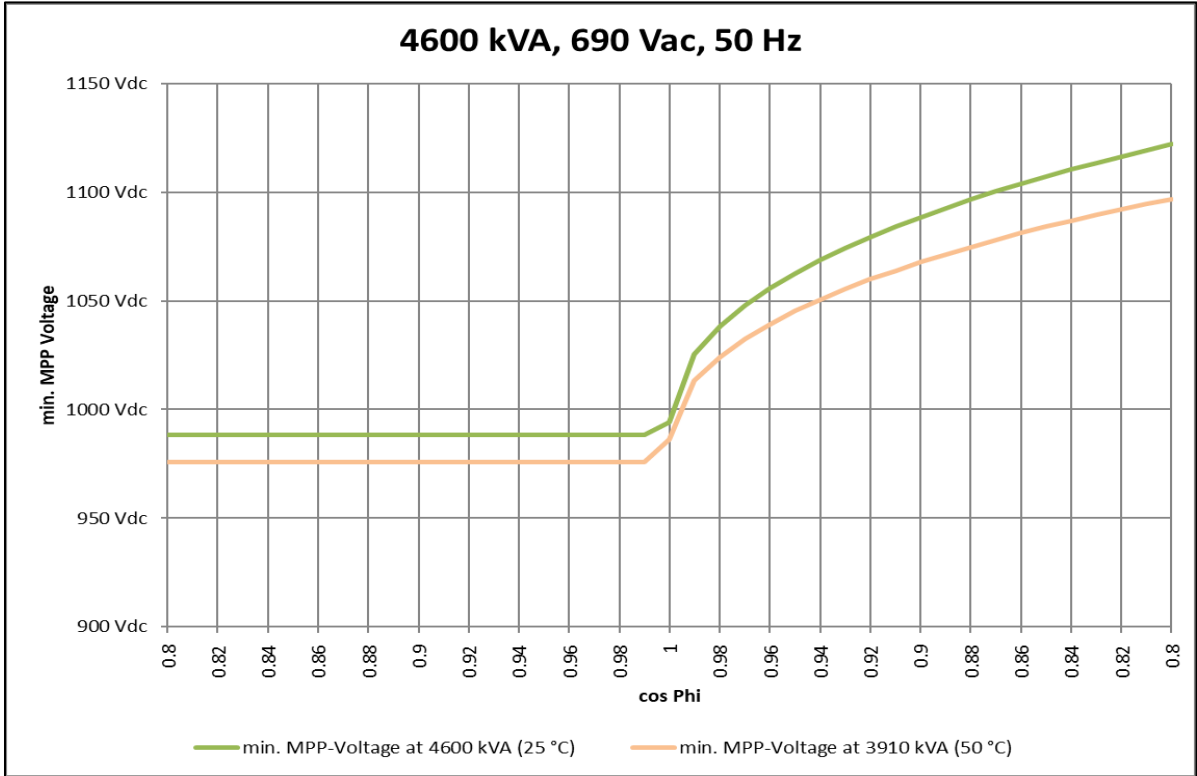**Figure 26: Minimum MPP Voltage of SC 4400 UP(-US) at 60 Hz**
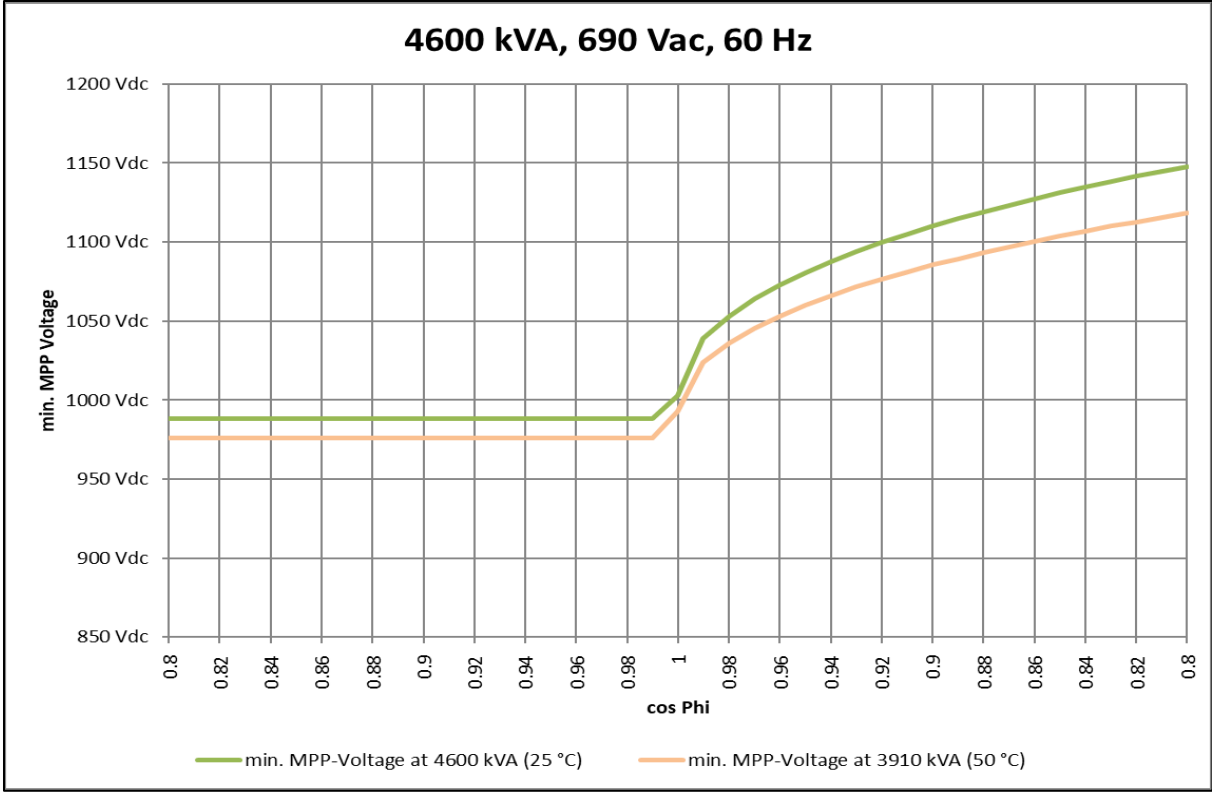
Figure 27: Minimum MPP Voltage of SC 4600 UP(-US) at 60 Hz

e) Minimum MPP Voltage with reactive power @50 Hz

Figure 28: Minimum MPP Voltage of SC 4000 UP(-US) at 50 Hz

Figure 29: Minimum MPP Voltage of SC 4200 UP(-US) at 50 Hz

Figure 30: Minimum MPP Voltage of SC 4400 UP(-US) at 50 Hz

Figure 31: Minimum MPP Voltage of SC 4600 UP(-US) at 50 Hz

5. De-rating

The thermal management of the inverter decides about de-rating conditions in dependence of ambient temperature, DC voltage and altitude.

Above 25°C the output power of the inverter has to be reduced. High DC voltage causes switching losses at the IGBTs which significantly contribute to the heat rise inside the inverter. With rising ambient temperature the maximum operation DC voltage with full load needs to be reduced linearly between 25°C and 50°C in order to support the inverter's thermal management.

The lower density of air with rising altitude reduces the cooling effect. The inverter can produce its full power output at altitudes up to 3,000m with only reducing slightly the max. temperature for operation with nominal power. An adaptation starts above 1,000m and results in a linear shift to lower max. temperature also aligned with the temperature drop at high altitudes.
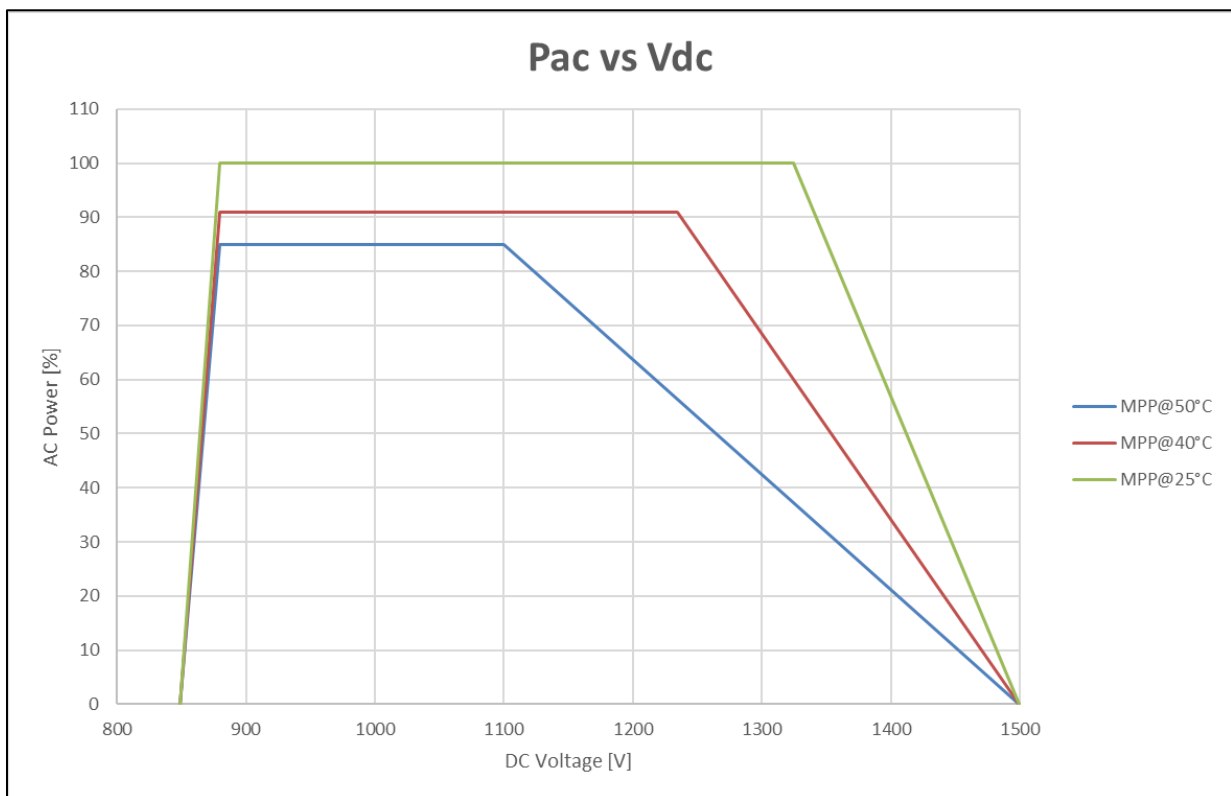
a) De-rating due to DC voltage

Figure 32: De-rating depending on DC voltage
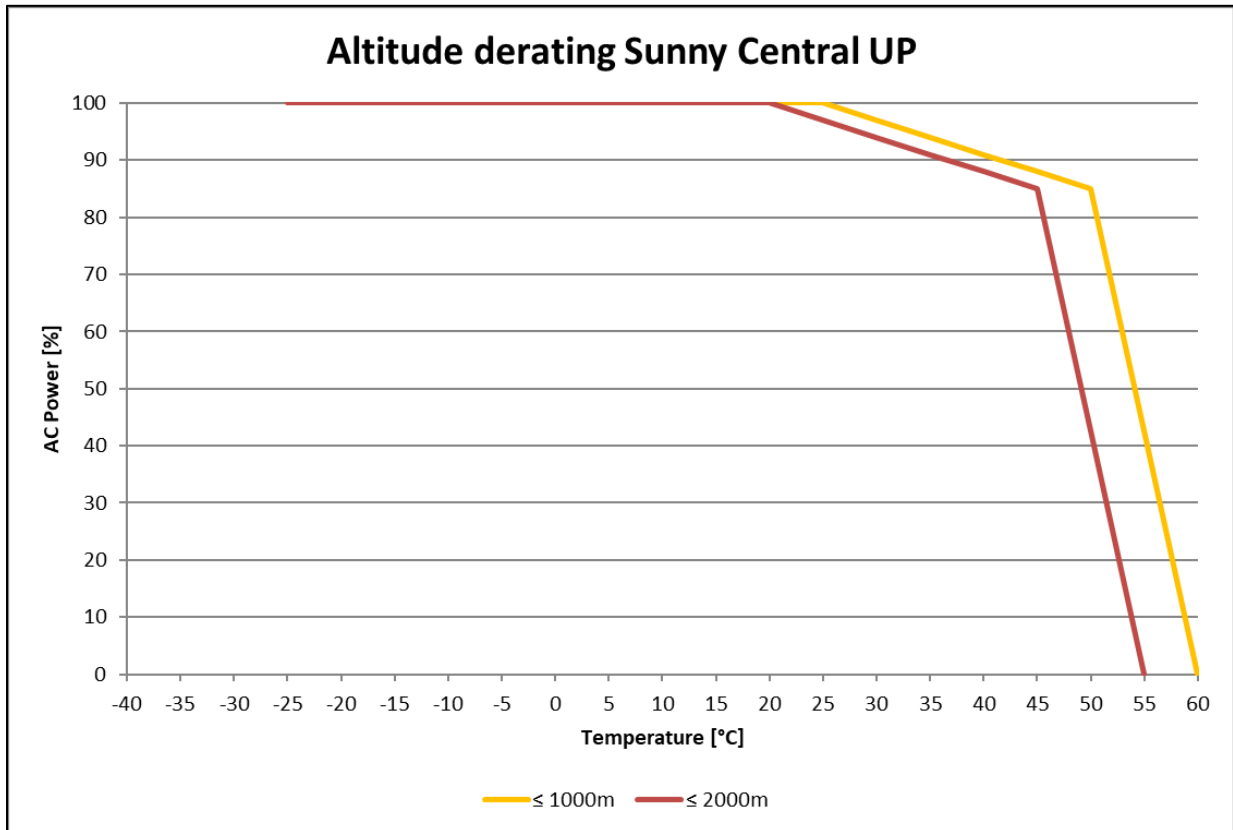
b) De-rating at high Altitudes

Figure 33: Linear de-rating at high altitudes

(Derating curves for altitudes above 2000m will be provided beginning of 2020)

6. Ride Through capabilities

The inverter has the capability to support the grid by remaining online or by reactive power feed-in during a temporary change of the grid voltage beyond preset low voltage (LV) and high voltage (HV) thresholds. The below figure describes the max. voltage ride-through (VRT) capabilities of the SC XXXX UP(-US). If the max. disconnecting delay time at specific voltage levels is exceeded, the inverter switches off and reconnects to the grid when the voltage returns to the preset nominal operation window.

A project specific VRT window can be defined with the parameters described in the inverter's operation manual.

The inverter will also ride through abnormal frequency events with the capability of reducing the output power at high frequency scenarios. The ride-through capabilities are described below with similar possibilities to adjust the window as for the voltage ride-through.
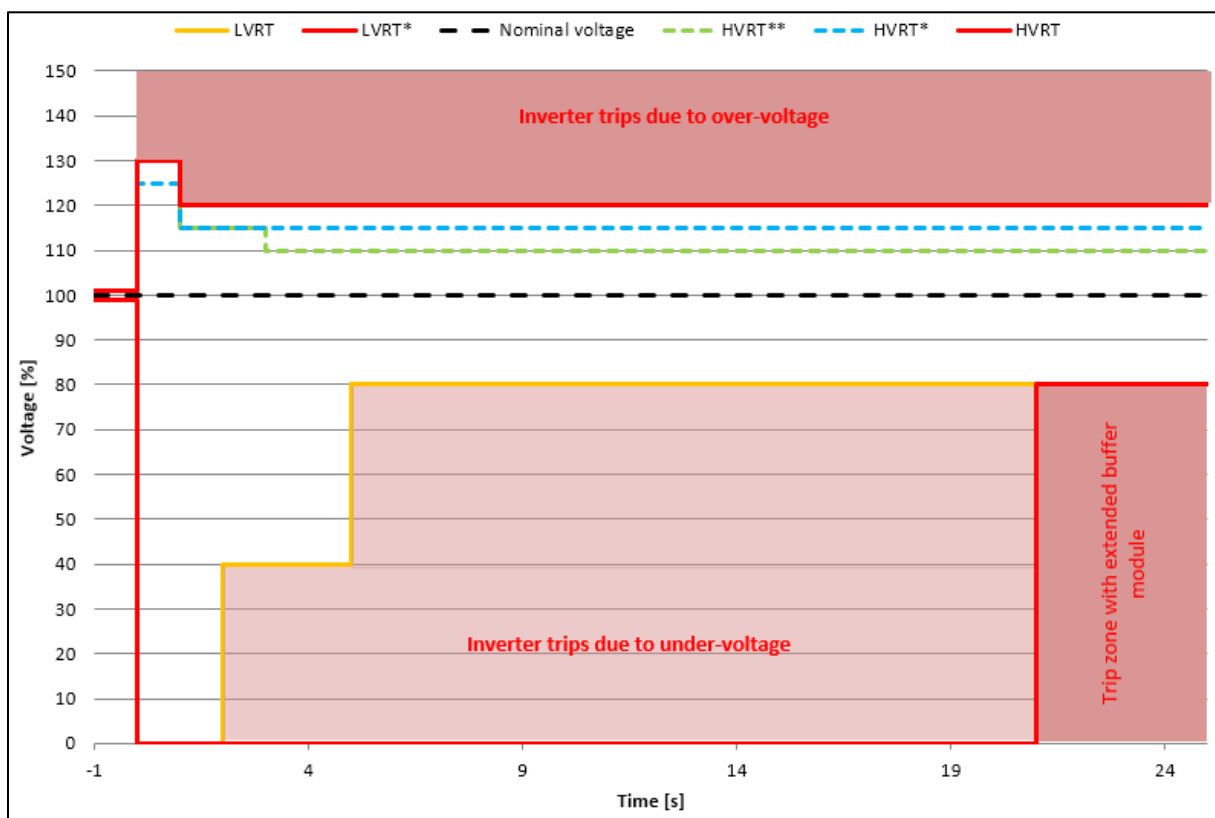
a) Voltage Ride Through

Figure 34: LVRT/HVRT capabilities

LVRT* → includes extended buffer module
HVRT* → SC 4400 UP(-US) → 2x 20 sec with 120%Un in 20 years allowed (esp. Australia)
HVRT** → SC 4600 UP(-US)
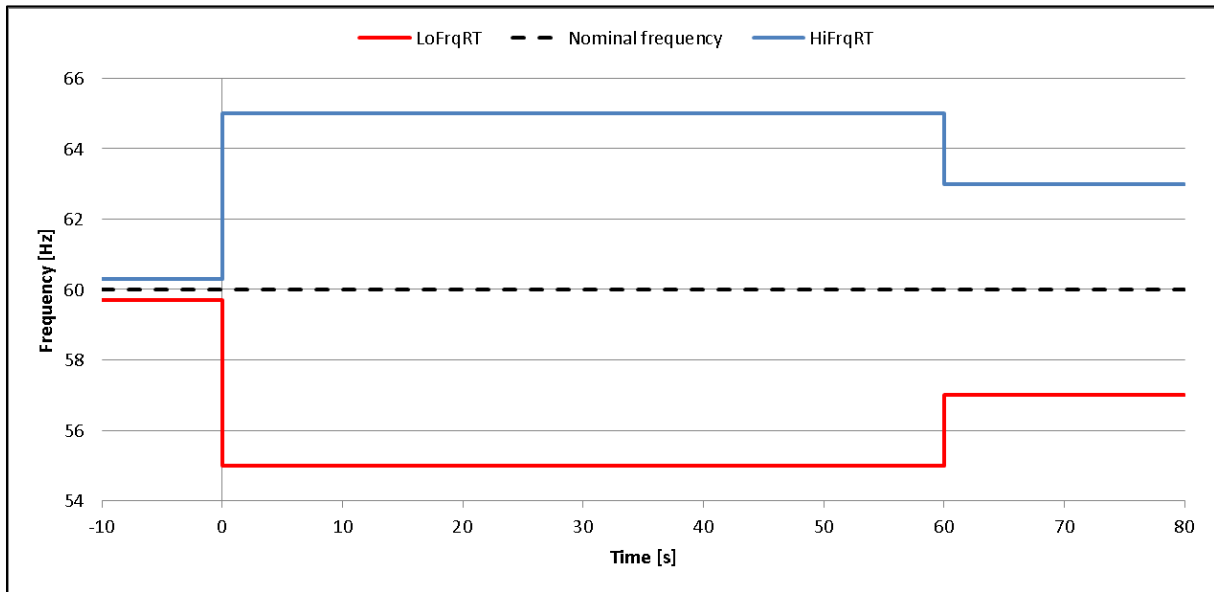
b) Frequency Ride Through
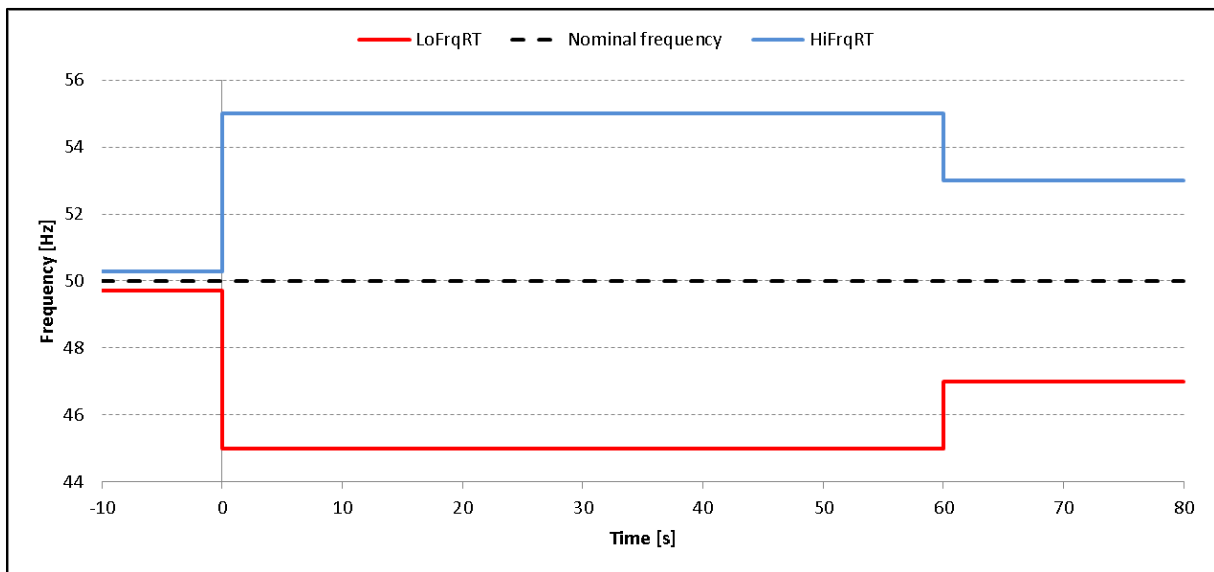

Figure 35: LoFrqRT/HiFrqRT capabilities (60 Hz)

Figure 36: LoFrqRT/HiFrqRT capabilities (50 Hz)

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